

Drax 11.6" Schematic

KBL-Y

2016-06-28

REV : A00

DY : None Installed

DRAX KBL Y



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Drax KBL Y

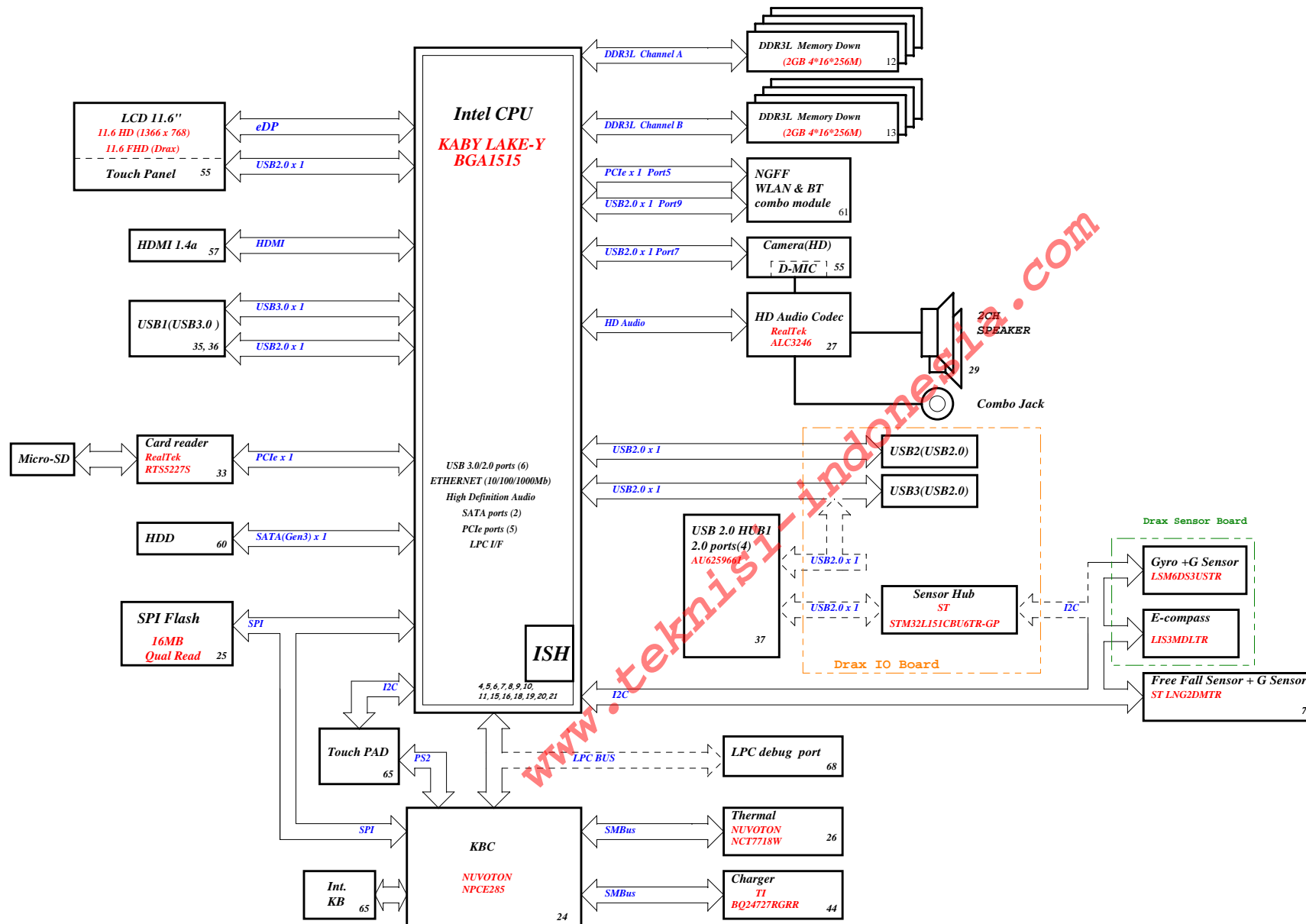
Rev
A00

Date: Tuesday, June 28, 2016

Sheet 1 of 109

Project code : 4PD06Q010001
PCB P/N : 16821
Revision : A00

Drax 11.6" Block Diagram



CHARGER	
BQ24727RGRR 44	
INPUTS	OUTPUTS
19V_DCBATOUT	12V_BT+
SYSTEM DC/DC	
SY8288CRAC 45	
SY8286BRAC	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5
	5V_PWR_2
	5V_S5
	3D3V_S5
CPU Core Power	
NCP81208MNTX6 46-50	
NCP81381MNTX6 *2	
SY8288RAC	
NCP81253MNTB6	
INPUTS	OUTPUTS
19V_DCBATOUT	+VCC_CORE
	+VCCGT
	1DOV_S5
	+VCCSA
DDR3L SUS	
SY8288RAC 51	
APL5338XAI	
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_S3
	0D675V_S0
SYSTEM DC/DC	
APL5930KAI 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

PCB LAYER	
L1:Top	L5:Signal
L2:Signal	L6:GND
L3:GND	L7:Signal
L4:Signal	L8:Bottom

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Block Diagram	
Drax KBL Y	
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D

C

B

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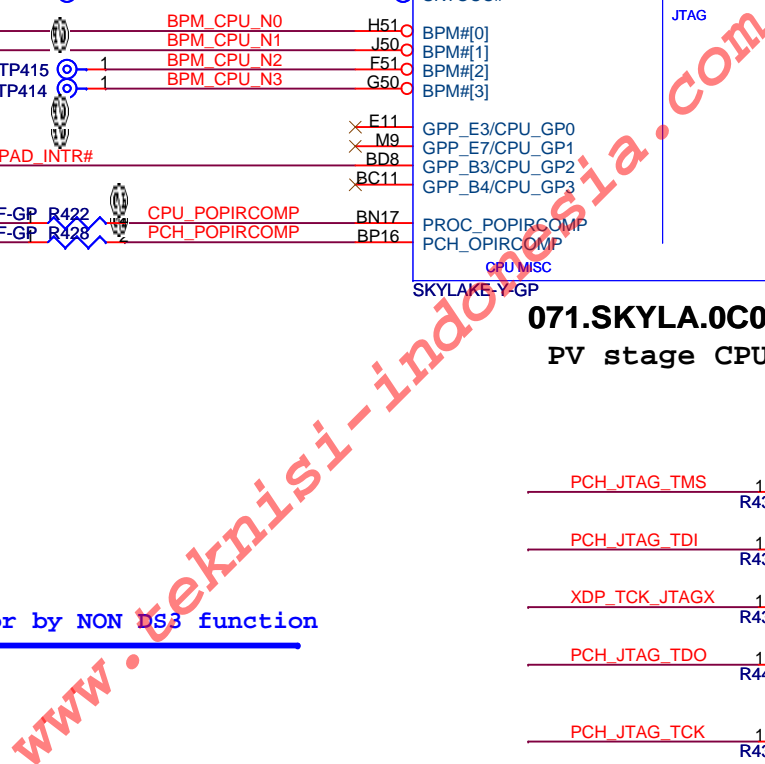
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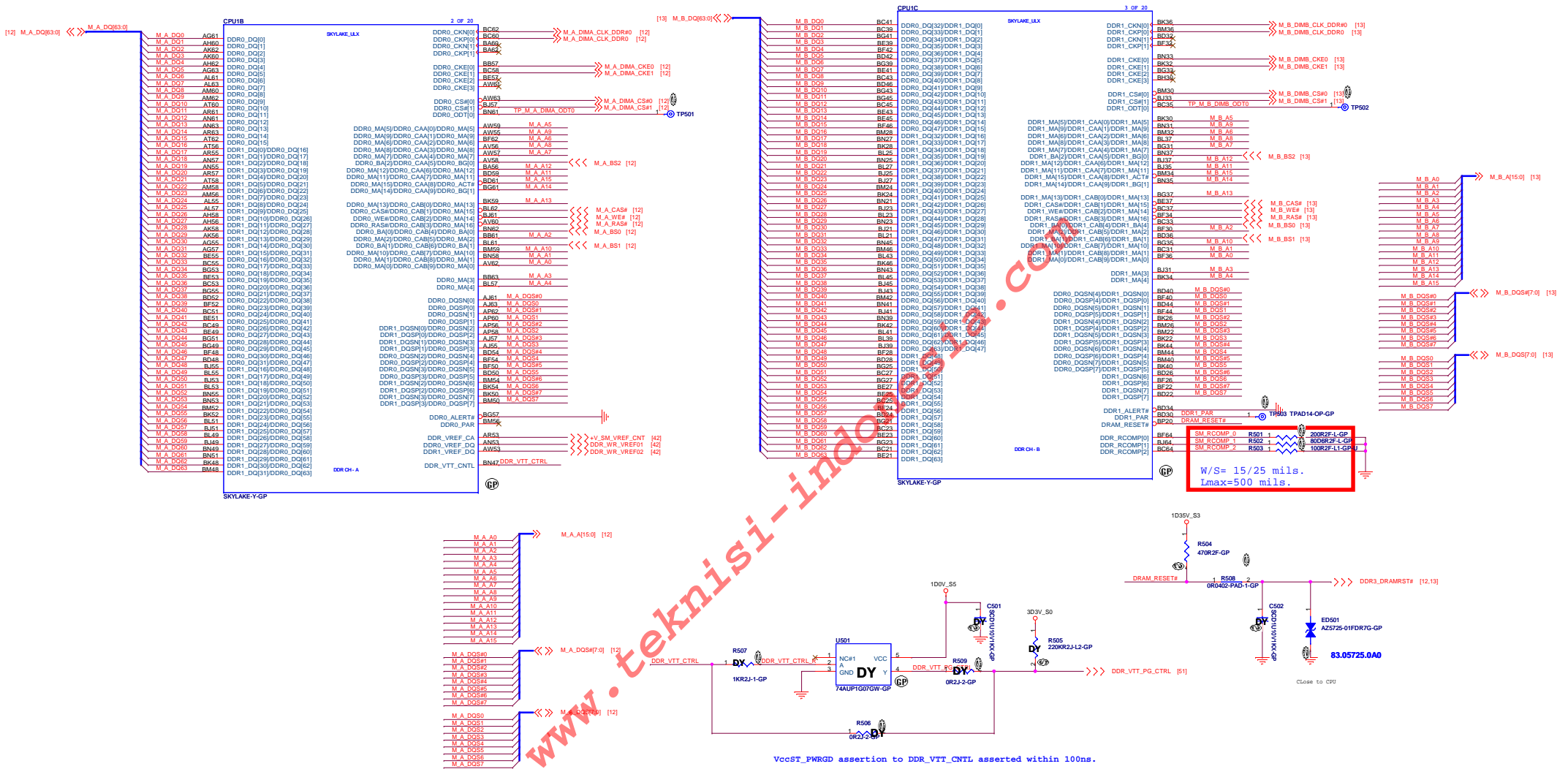
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Title					
Reserved					
Size	Document Number				Rev
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SSID = CPU



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Title CPU(DDR)			
Size A2	Document Number Drax KBL Y	Rev A00	
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SSID = CPU

[99] CFG[19:0]



CFG0	G52	CFG[0]
CFG1	F53	CFG[1]
CFG2	J52	CFG[2]
CFG3	H53	CFG[3]
CFG4	H55	CFG[4]
CFG5	D55	CFG[5]
CFG6	C56	CFG[6]
CFG7	F55	CFG[7]
CFG8	D61	CFG[8]
CFG9	G58	CFG[9]
CFG10	D57	CFG[10]
CFG11	F61	CFG[11]
CFG12	J60	CFG[12]
CFG13	J58	CFG[13]
CFG14	H61	CFG[14]
CFG15	H59	CFG[15]
CFG16	J54	CFG[16]
CFG17	G54	CFG[17]
CFG18	G56	CFG[18]
CFG19	J56	CFG[19]
CFG_RCOMP	A54	CFG_RCOMP
ITP_PMODE	A60	ITP_PMODE
B4	RSVD#B4	
B3	RSVD#B3	
F3	RSVD#F3	
F1	RSVD#F1	
L36	RSVD#L36	
L38	RSVD#L38	
BA19	RSVD#BA19	
BB18	RSVD#BB18	
BC19	RSVD#BC19	
BD18	RSVD#BD18	
D49	RSVD#D49	
M21	RSVD#M21	
L20	RSVD#L20	
M19	RSVD#M19	
L26	RSVD#L26	

CPU1T

20 OF 20

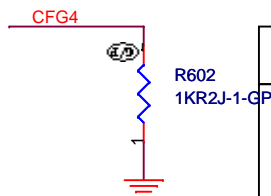
SKYLAKE_ULX

RSVD_TP#BL64	BL64
RSVD_TP#BG47	BG47
RSVD_TP#BA17	BA17
RSVD_TP#AY18	AY18
RSVD#BF18	BF18
RSVD#BE19	BE19
TP5	BA23
TP6	AY22
RSVD#R12	R12
RSVD#P13	P13
RSVD#M15	M15
RSVD#L16	L16
RSVD#L18	L18
RSVD#M17	M17
RSVD#AH7	AH7
RSVD#K12	K12
RSVD#H12	H12
RSVD#BN3	BN3
RSVD#BP3	BP3
RSVD#L22	L22
RSVD#M23	M23
TP4	BN1
RSVD#AY20	AY20
RSVD#BA21	BA21
RSVD#BB14	BB14
RSVD#M25	M25
RSVD#L24	L24
RSVD#L28	L28
RSVD#M27	M27
TP1	BJ15
TP2	BJ17

RESERVED SIGNALS

SKYLAKE-Y-GP

PCH strap pin:



DISPLAY PORT PRESENCE STRAP

CFG[4]

0 : ENABLED
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
1 : DISABLED
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title

CPU (CFG/RSVD)

Size
A4

Document Number

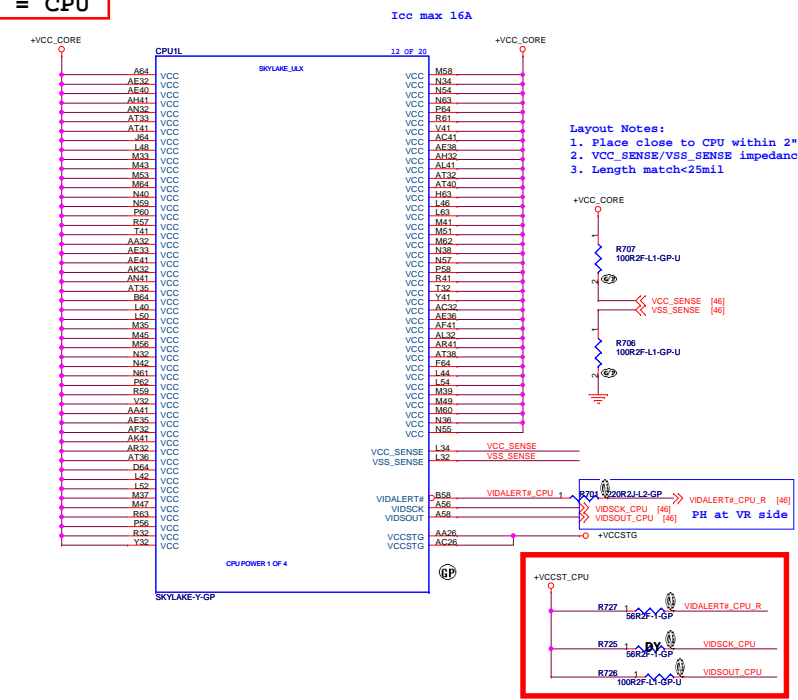
Drax KBL Y

Rev
A00

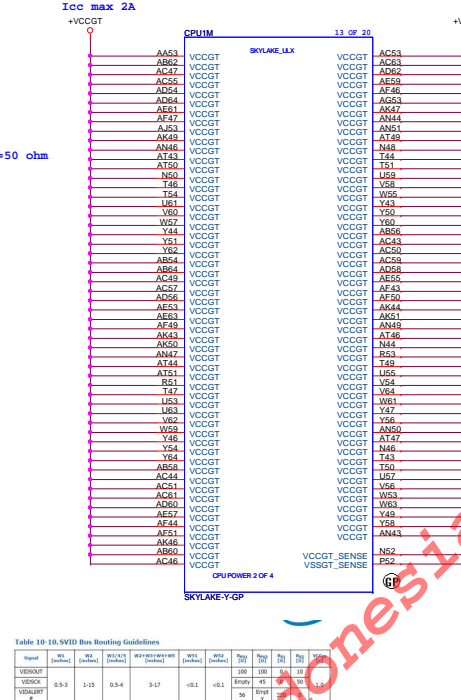
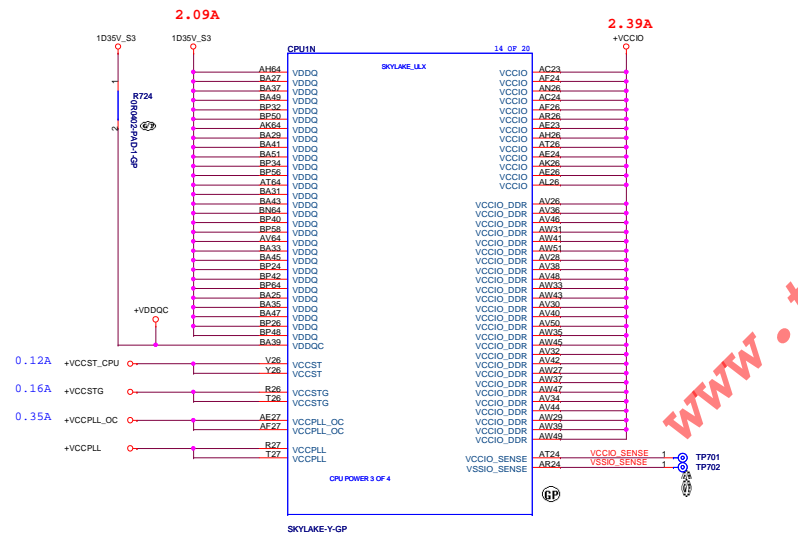
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SSID = CPU



- Layout Notes:
1. Place close to CPU within 2"
 2. VCC_SENSE/VSS_SENSE impedance=50 ohm
 3. Length match<25mil



- Layout Notes:
1. Place close to CPU within 2"
 2. VCCSTG_SENSE/VSSSTG_SENSE impedance=50 ohm
 3. Length match<25mil

Table 19-10: SVID Bus Routing Guidelines

Signal	VR (mm)	VR (mm)	VR (mm)	VR (mm)	VR (mm)	VR (mm)	VR (mm)	VR (mm)	VR (mm)
VDDQ	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	50
VDDQ	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	50

Note: For additional information regarding SVID and power management, please refer to Chapter 53, "Power Architecture" in this document.

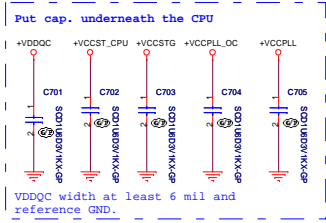
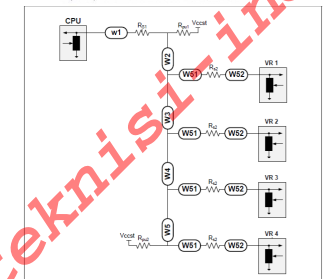
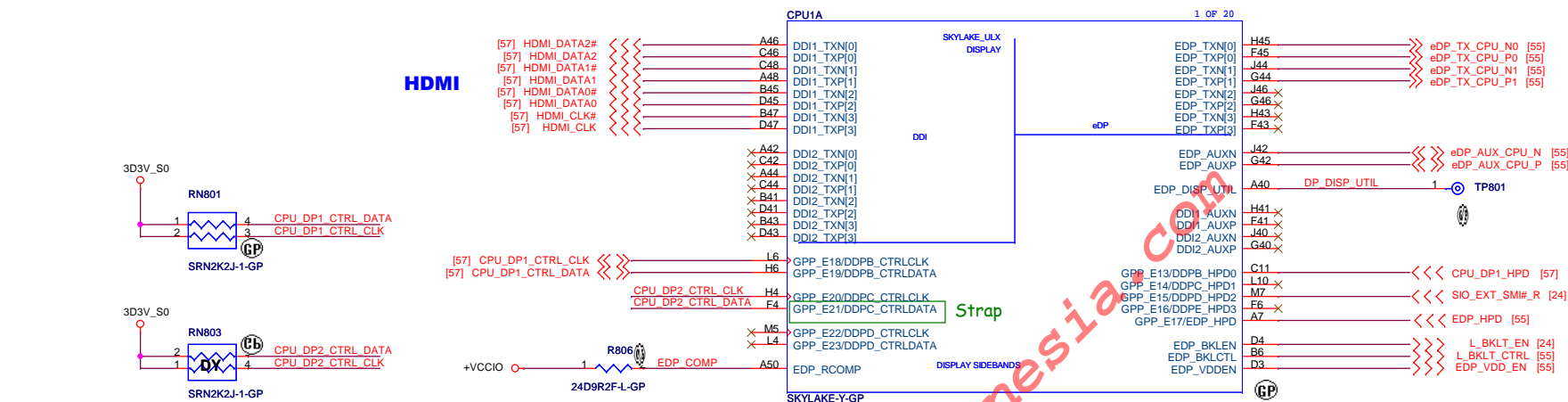


Table 52-2. Decoupling Requirements for Skylake Y Processor (Sheet 2 of 4)

Domain	Backside Cap	Primary Side Cap	Placement Guideline
VDDQC	1x 0.1 uF 0201		Filter implemented between VDDQC and VDDQ. Capacitor tapped directly to VDDQC first and connect to VDDQ through L (routed as trace). Please refer to Figure 66-6 for details.
VCCSA_DDR	1x 0.1 uF 0201		Place on secondary side, underneath the package. Refer to Note 4 for component placement.
VCCPLL_OC	1x 0.1 uF 0201	1x 22 uF 0603	Place as close to the package as possible.
VCCPLL	1x 0.1 uF 0201		Place on secondary side, underneath the package. Please refer to Figure 52-4 below.
VCCST ⁷	1x 0.1 uF 0201		Do not route VCCPLL, VCCST, VCCSTG closest adjacent layer over any power net other than ground.
VCCSTG ⁸	1x 0.1 uF 0201		Do not route VCCPLL, VCCST, VCCSTG closest adjacent layer over any power net other than ground.

SSID = CPU



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Design Guideline:

Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.

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File CPU (DISPLAY)			
Size A3	Document Number Drax KBL Y	Date: Tuesday, June 28, 2016	
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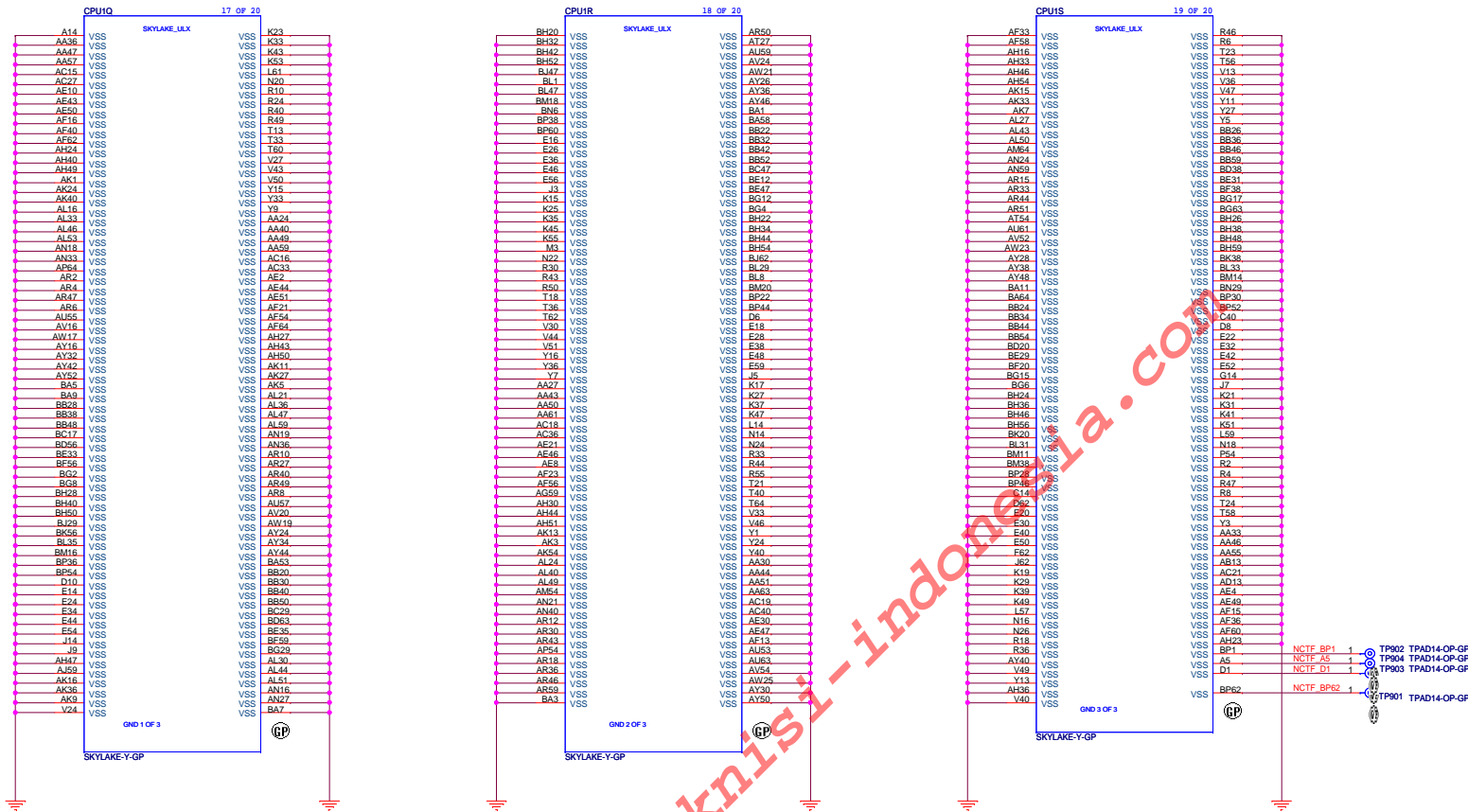
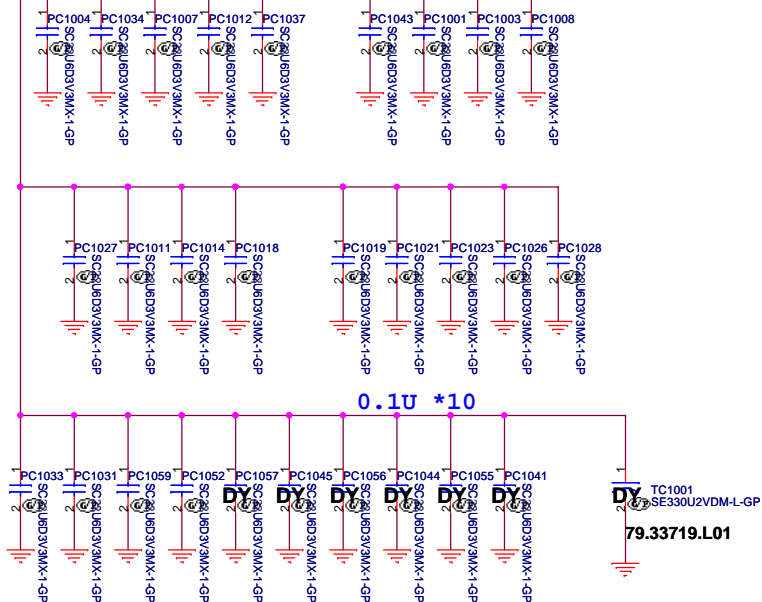


Table 45-3. Skylake Y Processor Corner NCTF Motherboard Test Point Example

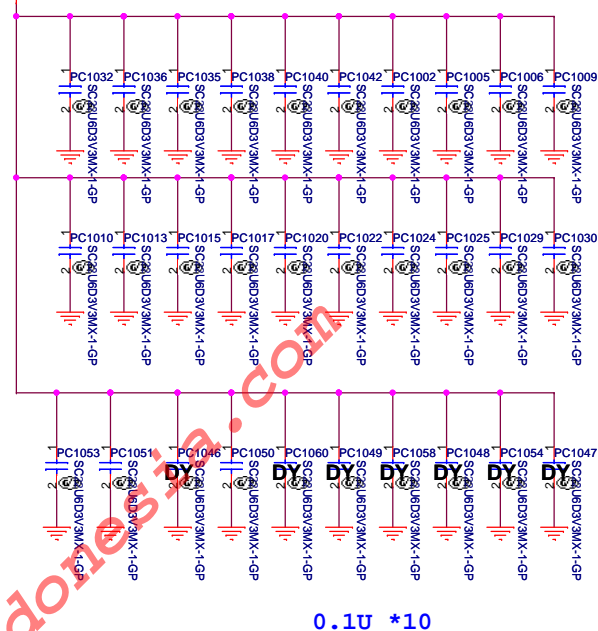
Pin Number	Pin Name	Description	Corner
BP64	NCTFVDDQ	Test Point (TP)	Corner BP64
BN64	NCTFVDDQ	Test Point (TP)	
BP62	NCTFVSS	Test Point (TP)	
BP1	NCTFVSS	Test Point (TP)	Corner BP1
D1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	Corner A64
A64	NCTFVCC	Test Point (TP)	
B64	NCTFVCC	Test Point (TP)	

Note: Refer to Processor EDS for more details on NCTF information.

+VCC_CORE 0603 update 22 uf cap *30(6DY)20151021 by PWR SKY



+VCCGT 0603 update 22 uf cap *30(6DY)20151021 by PWR SKY

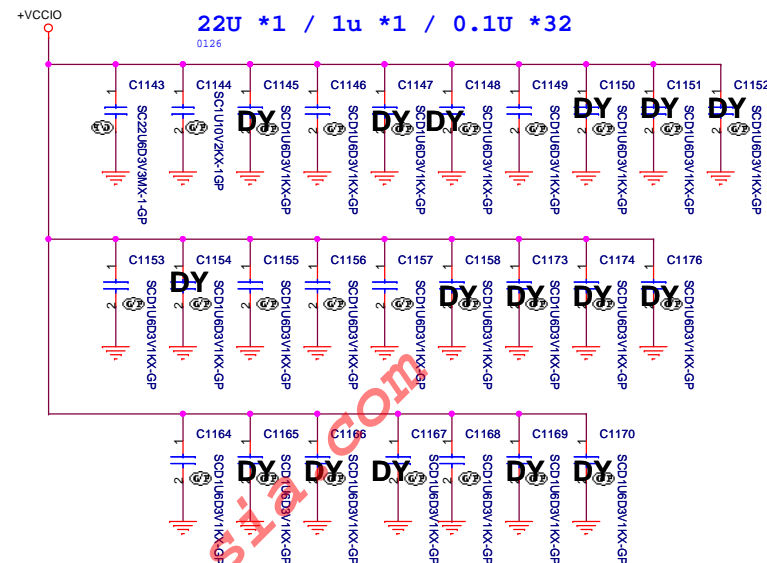
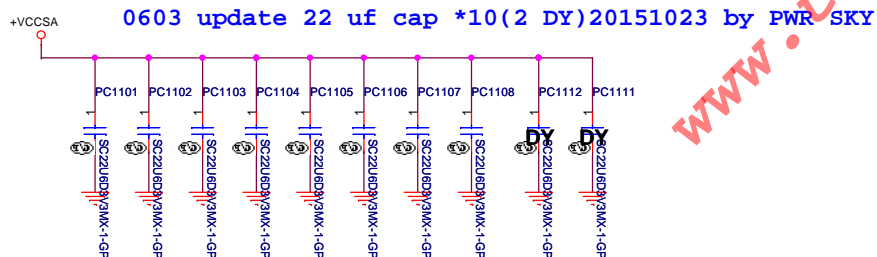
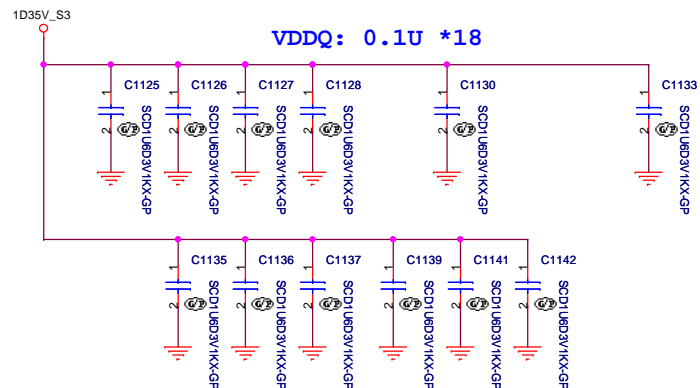
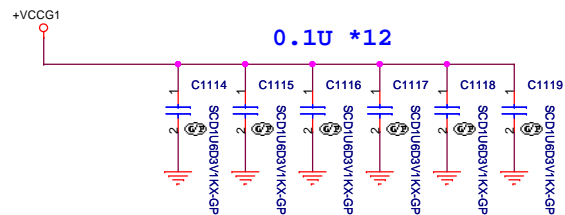
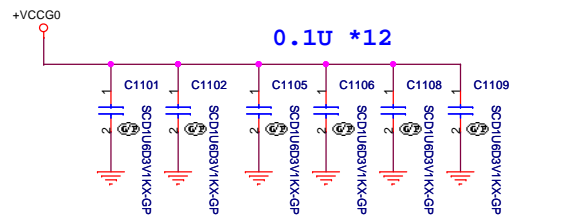


Decoupling Requirements for SKL Y Processor (Sheet 1 of 4)

Domain	Backside cap	Primary side cap	Placement guideline
VCCGT	12x 0.1uF 0201		Place on secondary side, underneath the package
	40x 0.1uF 0201 (Placeholder)		Refer to Note 2 for component placement
		2x 1uF 0402	Place as close to the package as possible.
		2x 10uF 0402 (Placeholder)	Placement order: Package edge > 0402 1uF caps > 0402 10uF caps > 0805 caps > Power source
		9x 47uF 0805 (6.3V) ¹	
Vcc	20x 0.1uF 0201		Place on secondary side, underneath the package
	12x 0.1uF 0201 (Placeholder)		Refer to Note 3 for component placement
		8x 10uF 0402	Place as close to the package as possible.
		6x 47uF 0805 (6.3V) ¹	Placement order: Package edge > 0402 caps > 0805 caps > Power source
		2x 47uF 0805 (Placeholder)	

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Title			
CPU (Power CAP1)			
Size	Document Number	Rev	
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Decoupling Requirements for Skylake Y Processor (Sheet 2 of 4)

Domain	Backside Cap	Primary Side Cap	Placement Guideline
V _{CCG0}	12x 0.1 uF 0201		Place on secondary side, underneath the package
V _{CCG1}	12x 0.1 uF 0201		Place on secondary side, underneath the package
V _{DDQ}	18x 0.1 uF 0201		Place on secondary side, underneath the package
V _{DDQC}	1x 0.1 uF 0201		Filter implemented between VDDQC and VDDQ. Capacitor tapped directly to VDDQC first and connect to VDDQ through L (routed as trace). Please refer to Figure 66-6 for details.
V _{CCIO}	13x 0.1 uF 0201		Isolation between DDR and display area. Place on secondary side, underneath the package Please refer to Figure 52-1 below
		1x 1 uF 0402	Place as close to the package as possible. Placement order: Package edge > 0402 caps > 0805 caps > Power source
V _{CCSA}	1x 1 uF 0201		Place on secondary side, underneath the package Refer to Note 4 for component placement Please refer to Figure 52-3 below
		4x 22 uF 0603	Place as close to the package as possible

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Title: **CPU (Power CAP2)**

Size: A3 Document Number: **Drax KBL Y** Rev: **A00**

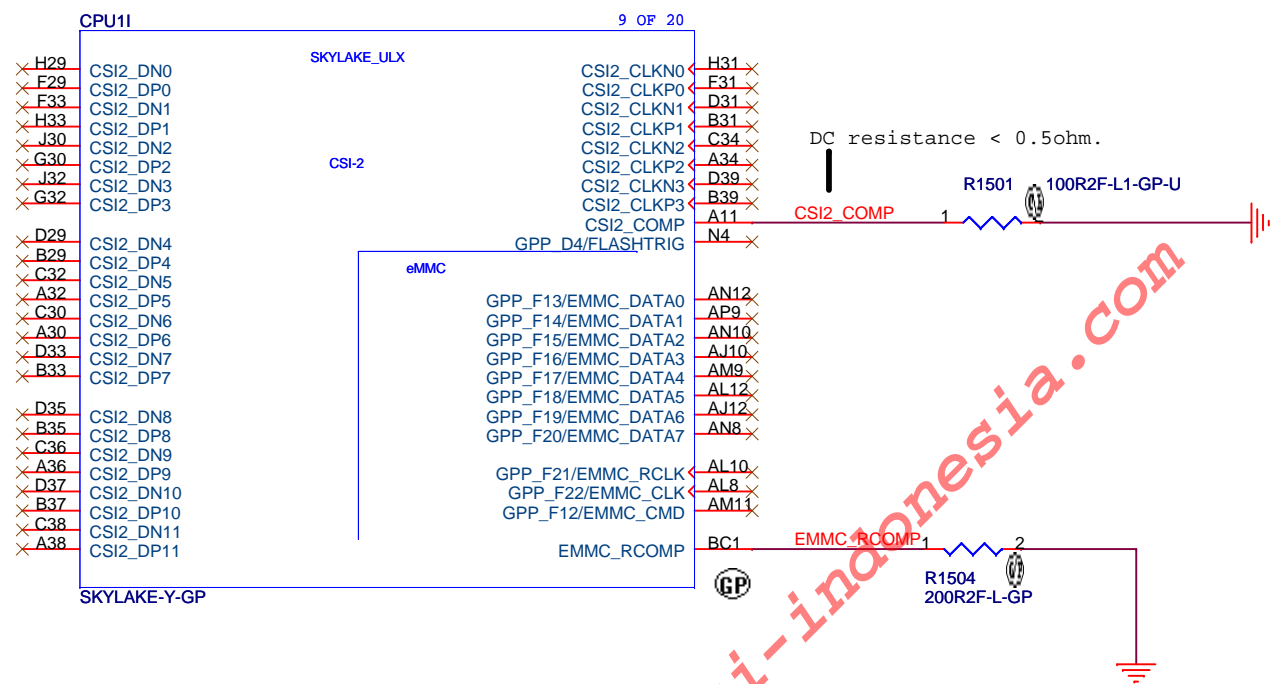
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Title CPU (CSI2/EMMC)			
Size A4	Document Number Drax KBL Y		Rev A00
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SSID = PCH

USB Table

Pair	Device
1	USB3.0 on MB
2	USB 2.0 on DB
3	USB 2.0 on DB
5	CAMERA
7	CAMERA
9	WLAN

WLAN

Card Reader

HDD

USB3.0 on MB

TOUCH SCREEN

CAMERA

USB2.0 on DB

WLAN

USB2.0 on DB

DC resistance < 0.5ohm.

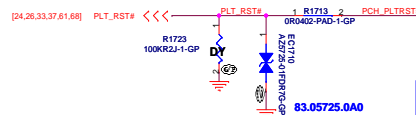
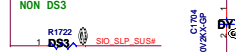
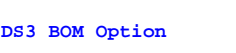
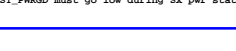
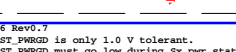
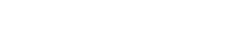
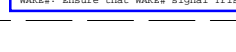
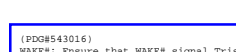
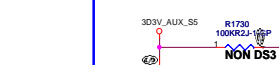
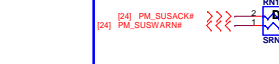
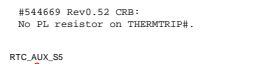
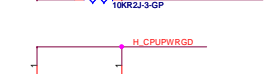
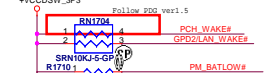
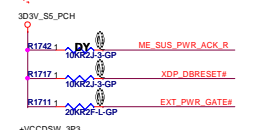
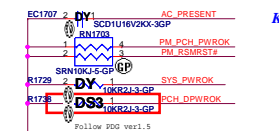
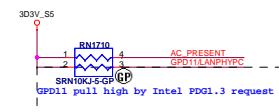
(#543611)

The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

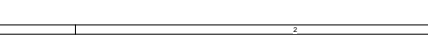
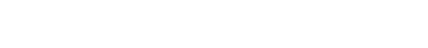
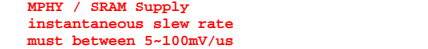
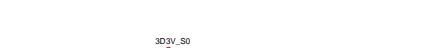
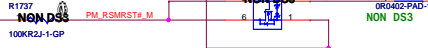
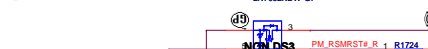
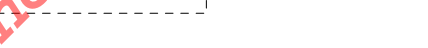
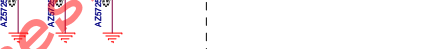
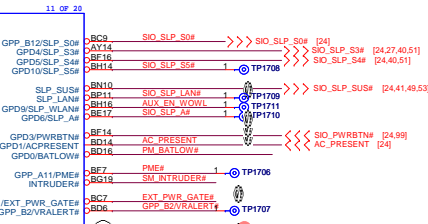
DRAX KBL Y

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU (PCIE/SATA/USB)			
Size: A3	Document Number: Drax KBL Y	Rev: A00	
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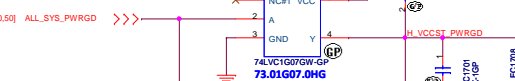
[B543016 Rev0.7]
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Layout note: 3 PAD SHARING



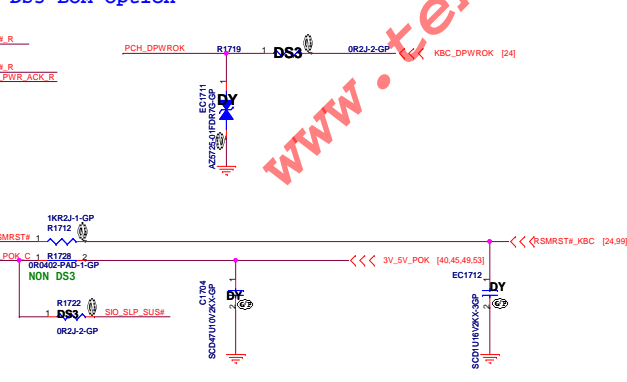
KBC delay 99ms

(PDG#543016)
WAKE# Ensure that WAKE# signal Trise (Maximum) is <100 ns.

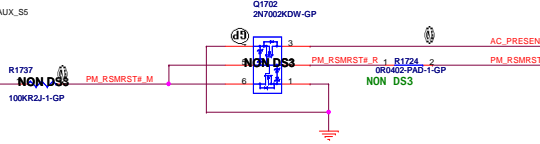


#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

DS3 BOM Option



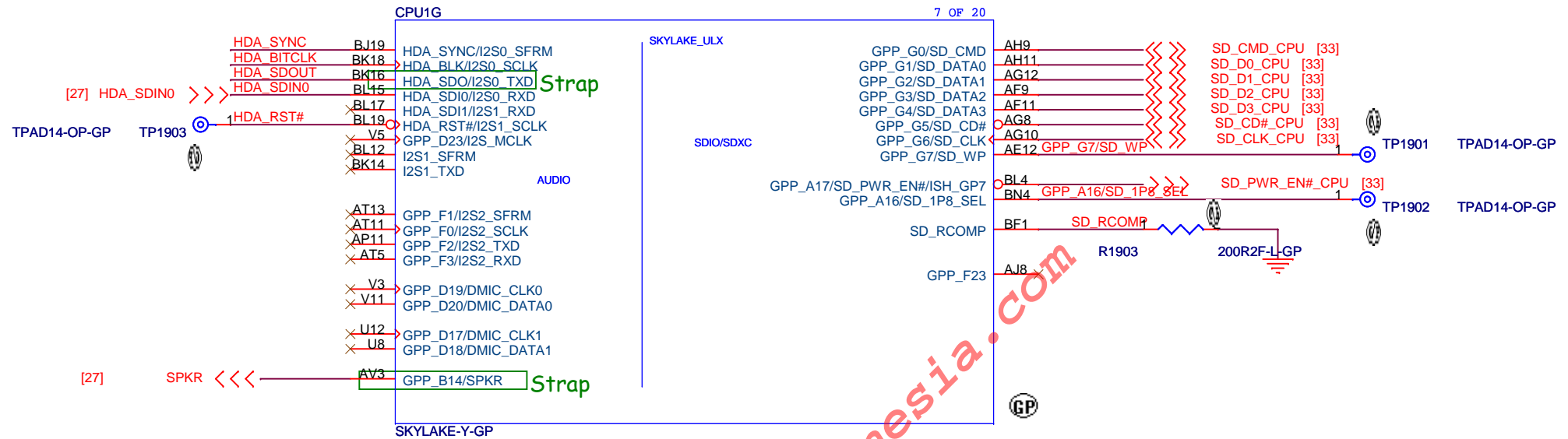
4th = 84.000000.03F
3rd = 75.000000.07C
2nd = 84.2N702.E3F
1st = 84.2N702.A3F



MPHY / SRAM Supply
instantaneous slew rate
must between 5-100mV/us
Tr between 10-200us

DRAX KBL Y

SSID = PCH



PCH strap pin:

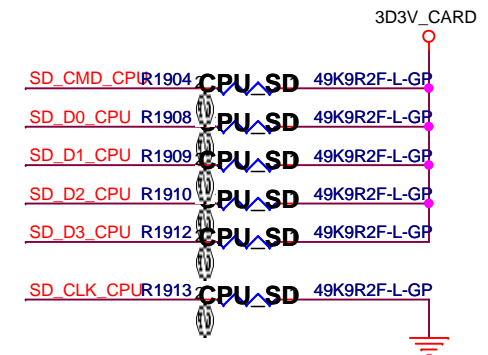
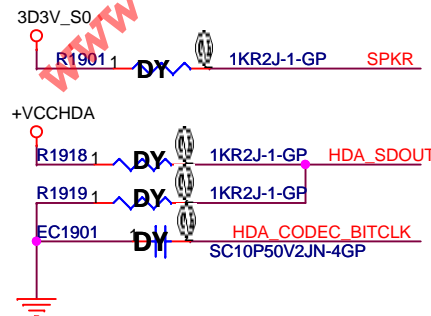
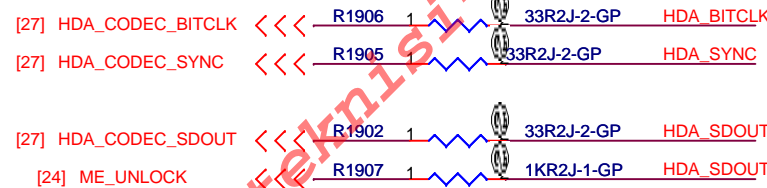
NO REBOOT	
HDA_SPKR	Low = Enable (Default) * High = Disable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDO	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts



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Title					
CPU (AUDIO/SDIO)					
Size	Document Number		Rev		
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Vender	RAM ID	Wistron PN	Mfr. PN	Capacity	Freq
Micron	X000	NX80R\$CB	MT41K256M16LY-107:N	2G	1600MHz
Hynix	X001	NX80R\$AB	H5TC4G63CFR-PBA	2G	1600MHz
Micron	X010	NX80R\$CC	MT41K256M16T	2G	1600MHz
Samsung	X011	NX80R\$BD	K4B4G1646E-BYK0	2G	1600MHz
Micron	X100	NX80R\$CB	MT41K256M16LY-107:N	4G	1600MHz
Hynix	X101	NX80R\$AB	H5TC4G63CFR-PBA	4G	1600MHz
Micron	X110	NX80R\$CC	MT41K256M16T	4G	1600MHz
Samsung	X111	NX80R\$BD	K4B4G1646E-BYK0	4G	1600MHz

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI (Default) High = LPC

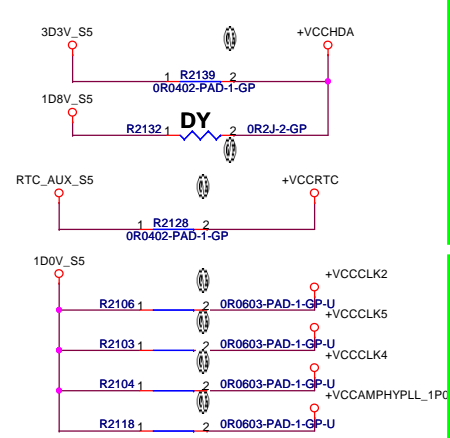
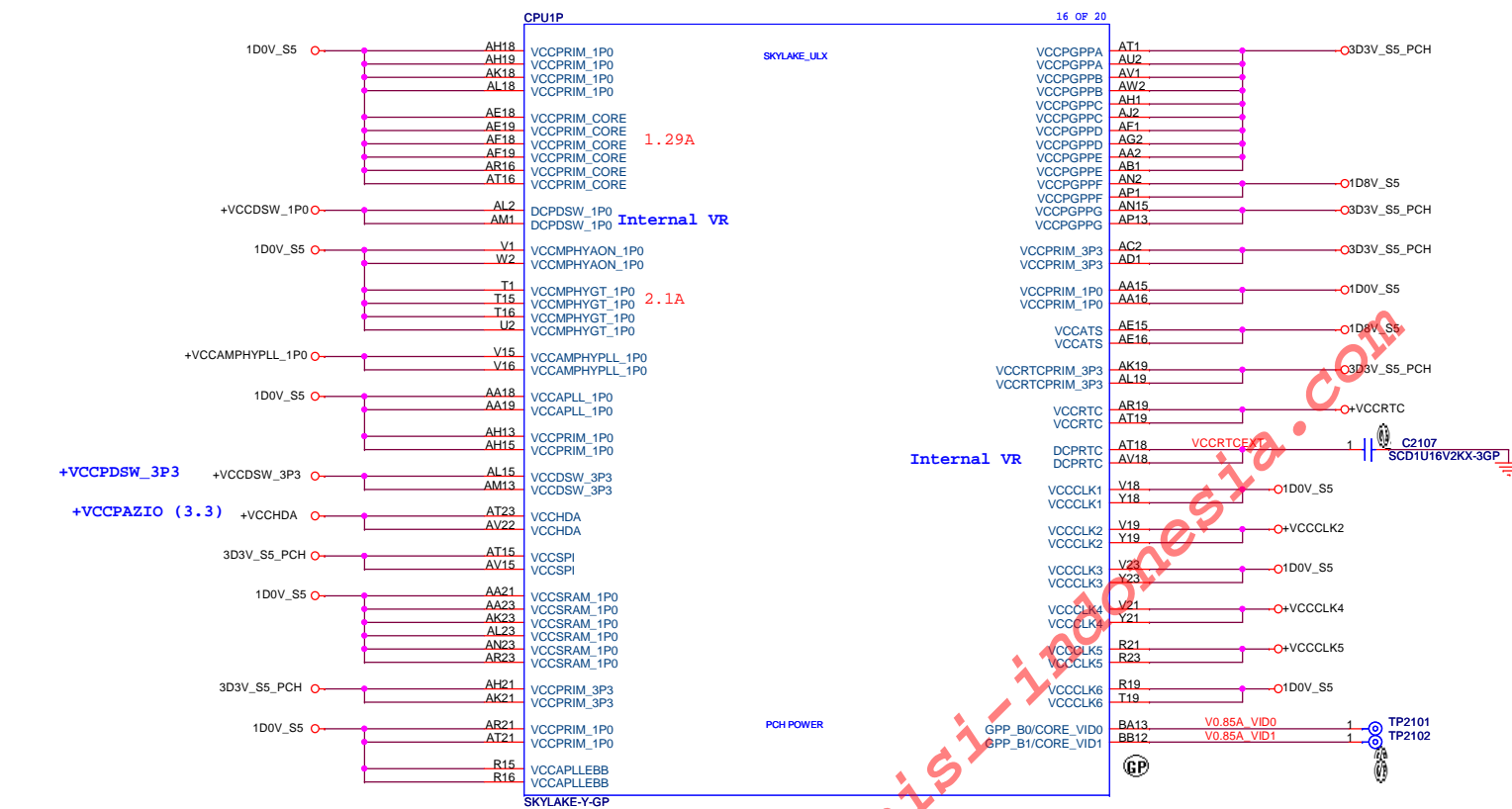
The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GPIO_MQSI / GPP_B18	<p>* 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p>

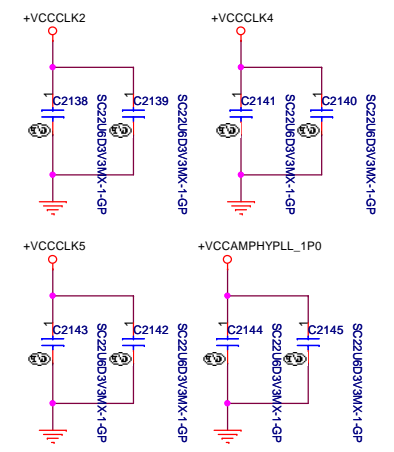
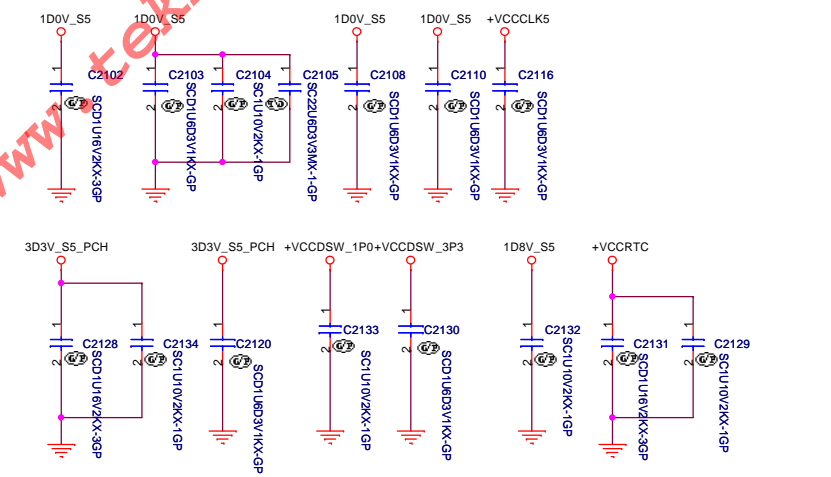
The signal has a weak internal pull-down.

SSID = PCH



Layout Note:
D1uF:
C2102 near V1
C2103 near T1, T15
C2108 near AH13, AH15
C2110 near R15, R16
C2116 near R21
1uF:
C2104 near T1, T15
22uF:
C2105 near T1, T15

Layout Note:
D1uF:
C2128 near AK19
C2120 near AT15
C2130 near AL15
C2131 near AR19
1uF:
C2134 near AK19
C2129 near AR19
C2132 near AE15
C2133 near AL2



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Size
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Document Number

Drax KBL Y

Rev

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Date: Tuesday, June 28, 2016

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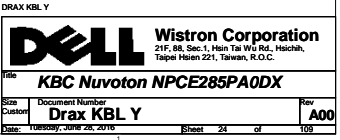


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SPI Flash ROM(16M) for PCH 3D3V_S5_PCH

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Title

Flash/RTC

Size
A3

Document Number

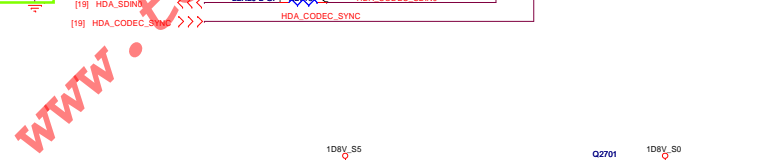
Drax KBL Y

Rev	A00
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Date: Tuesday, June 28, 2016

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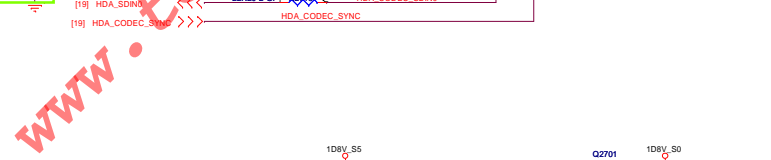
Timing diagram for HDA_CODEC_SYNC signal. The diagram shows a green square wave for 1D8V_S5 and a blue square wave for HDA_CODEC_SYNC. The HDA_CODEC_SYNC signal is active (high) during the period when 1D8V_S5 is high. The signal is labeled with [19] HDA_CODEC_SYNC and [19] HDA_CODEC_SYNC.



Timing diagram for HDA_CODEC_SYNC signal. The diagram shows a green square wave for 1D8V_S5 and a blue square wave for HDA_CODEC_SYNC. The HDA_CODEC_SYNC signal is active (high) during the period when 1D8V_S5 is high. The signal is labeled with [19] HDA_CODEC_SYNC and [19] HDA_CODEC_SYNC.

Timing diagram for HDA_CODEC_SYNC signal. The diagram shows a green square wave for 1D8V_S5 and a blue square wave for HDA_CODEC_SYNC. The HDA_CODEC_SYNC signal is active (high) during the period when 1D8V_S5 is high. The signal is labeled with [19] HDA_CODEC_SYNC and [19] HDA_CODEC_SYNC.

Timing diagram for HDA_CODEC_SYNC signal. The diagram shows a green square wave for 1D8V_S5 and a blue square wave for HDA_CODEC_SYNC. The HDA_CODEC_SYNC signal is active (high) during the period when 1D8V_S5 is high. The signal is labeled with [19] HDA_CODEC_SYNC and [19] HDA_CODEC_SYNC.



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Rev
A00

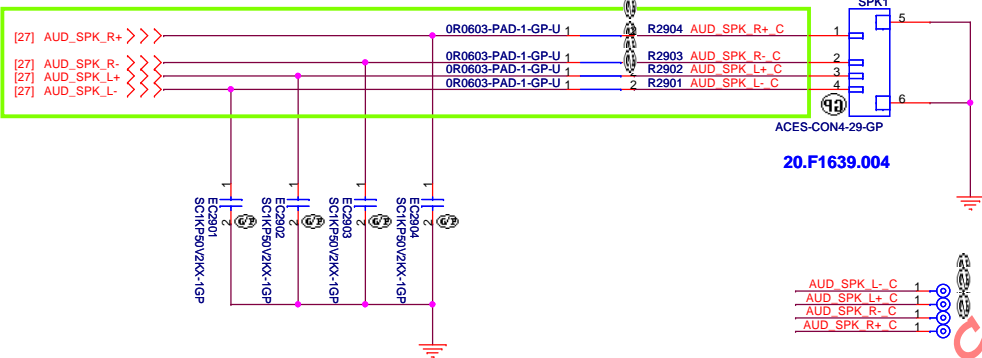
Date: Tuesday, June 28, 2016

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Main Func = Audio

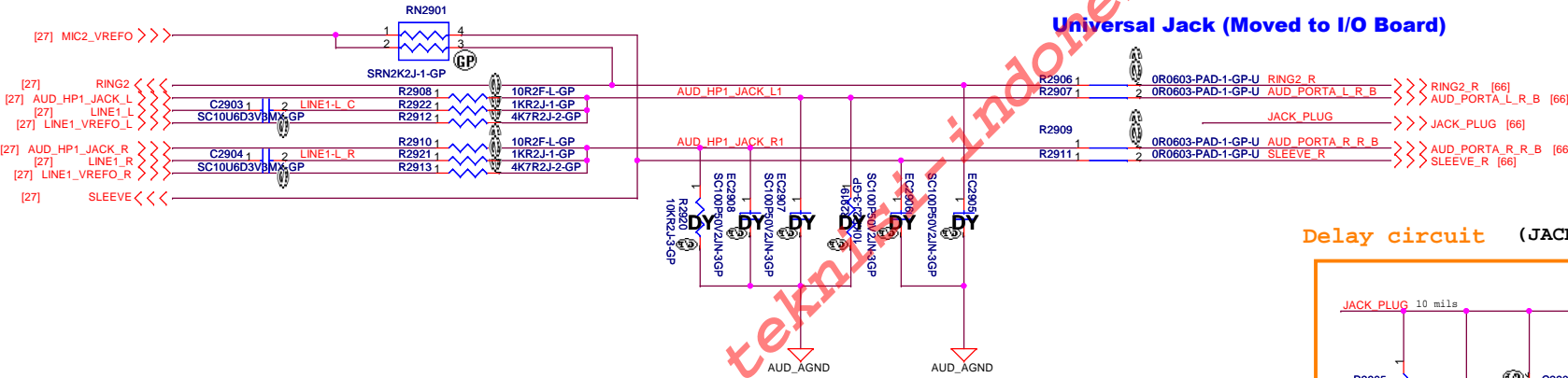
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

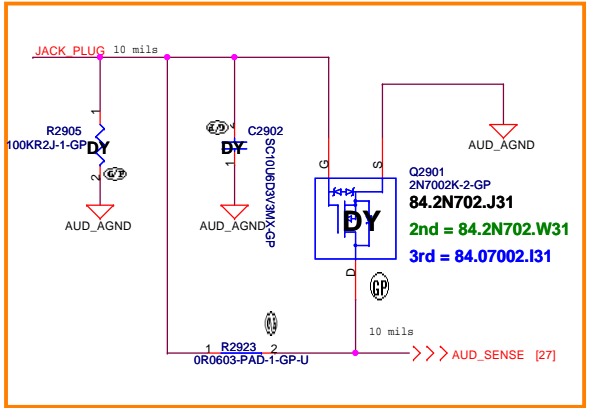


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Delay circuit (JACK_PLUG_DET: on IO Board)



SSID = LOM

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SSID = LAN

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Title (Reserved)LAN			
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SSID = LAN CONN

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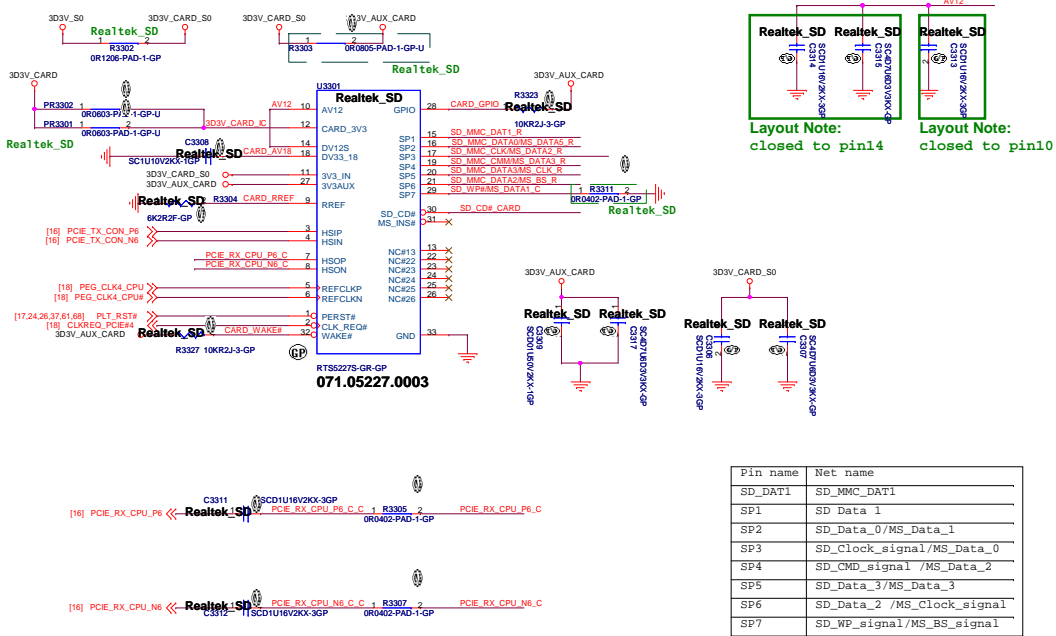
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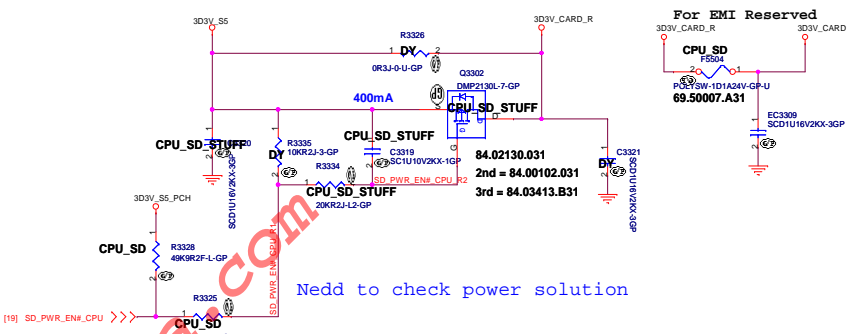
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)RJ45+Transformer					
Size A4		Document Number Drax KBL Y			Rev A00
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SSID = Card Reader

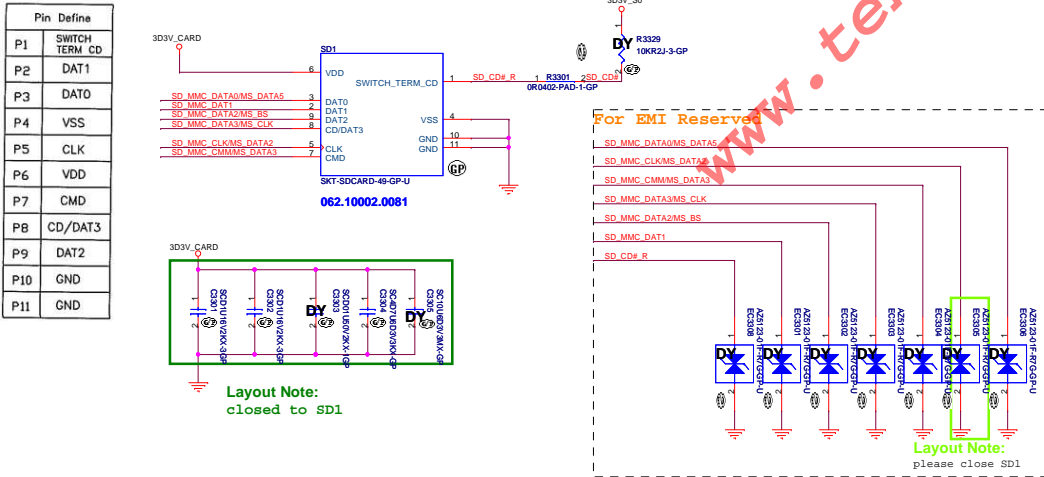
Card Reader IC (PCIE Interface)



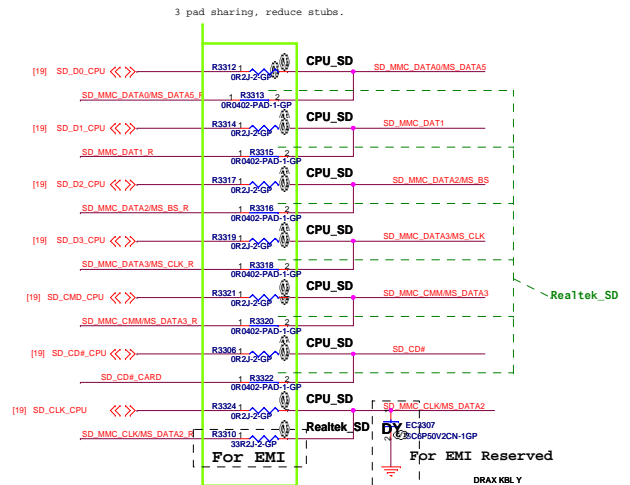
Card Reader Power SW (CPU Only)



SD Card Connector



Co-lay from CPU and Card Reader IC



SSID = USB

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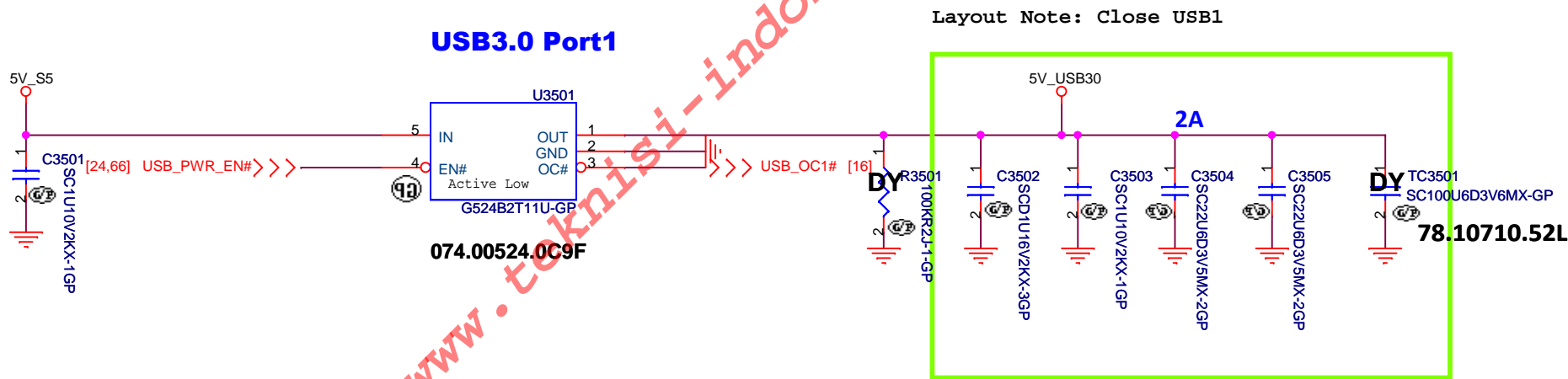


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Title **(Reserved)USB 2.0 Port**

Size A4	Document Number Drax KBL Y	Rev A00
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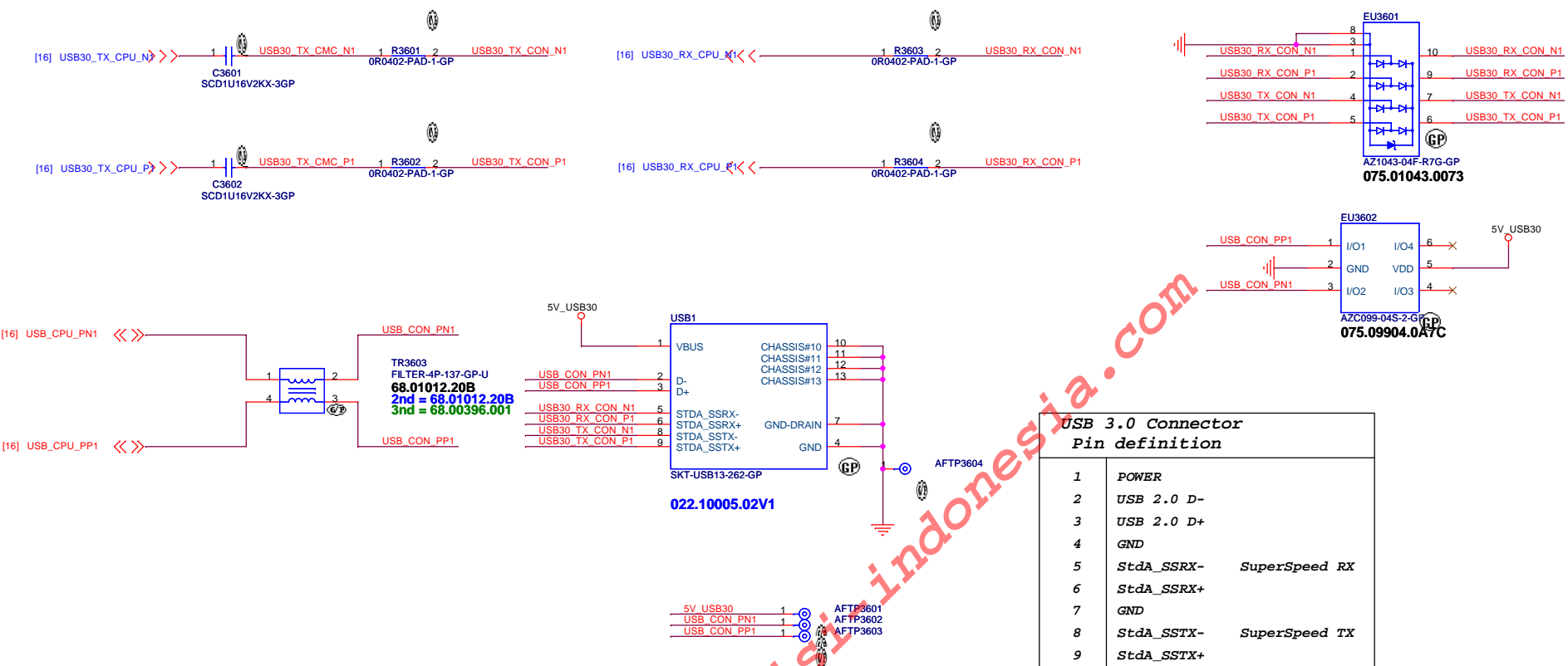
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Taipei Hsien 221, Taiwan, R.O.C.

Title
USB Power SW

Size A4	Document Number Drax KBL Y	Rev A00
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SSID = USB



USB 3.0 Connector	
Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

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Title

USB3.0 CONN

Size

Document Number

Rev

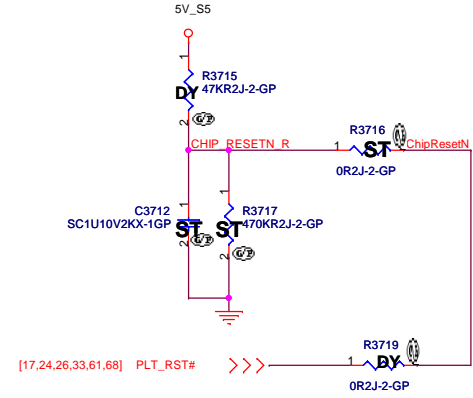
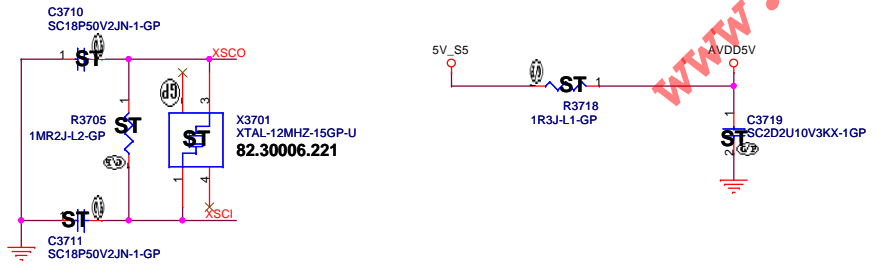
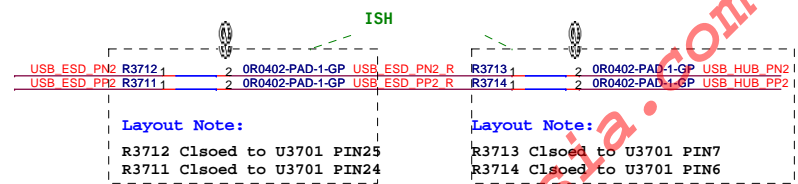
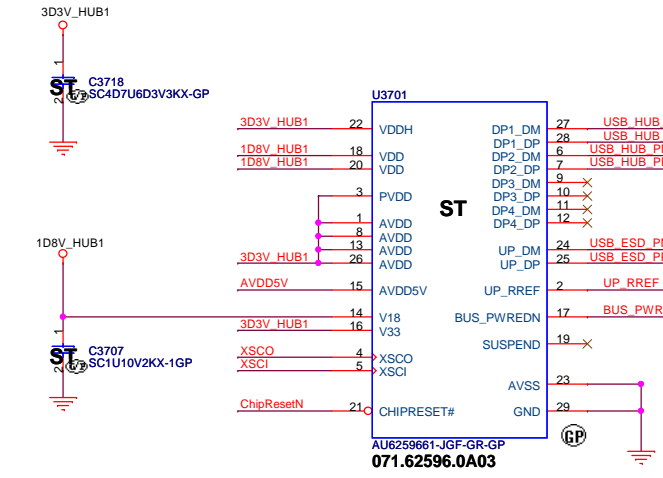
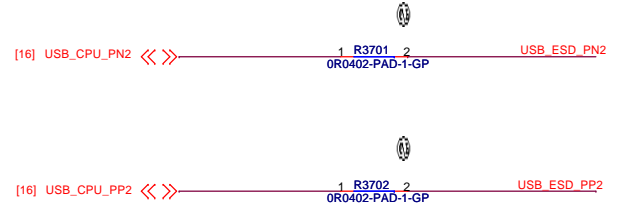
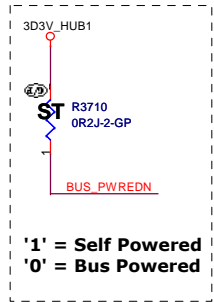
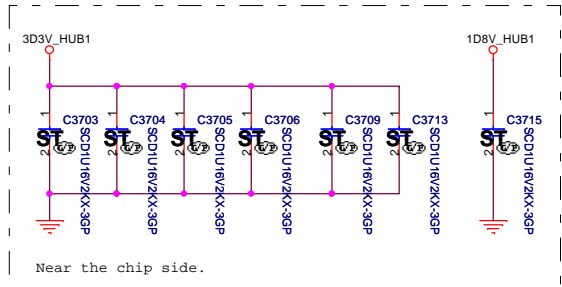
Drax KBL Y

A00

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SSID = USB



USB Table

Pair	Device
1	USB2.0 Port3
2	Sensor HUB
3	
4	

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Title

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A00


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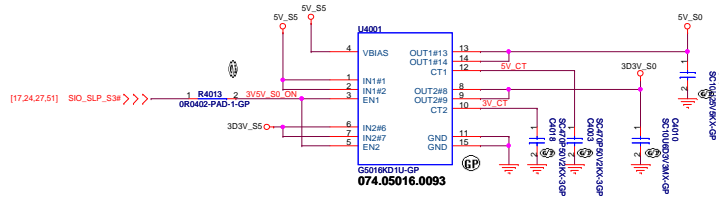
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ROSA Run Power



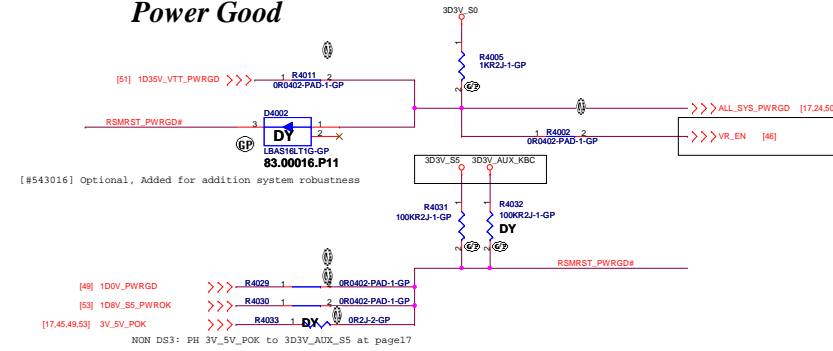
5V_S0

5V_S0 Consumption
Peak current 5A

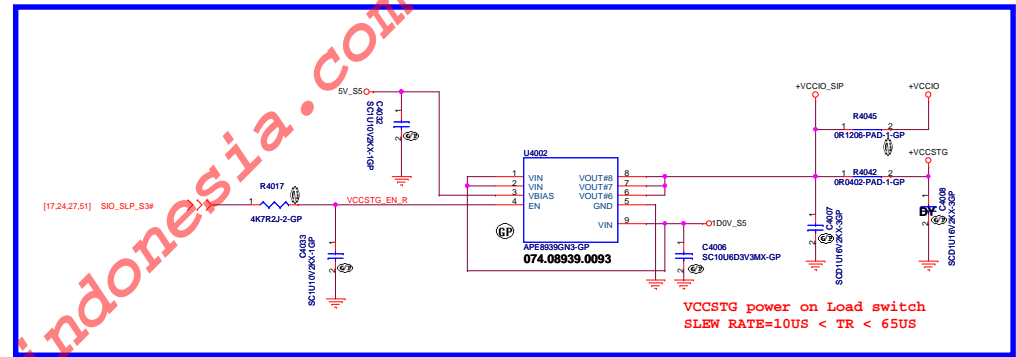
3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A

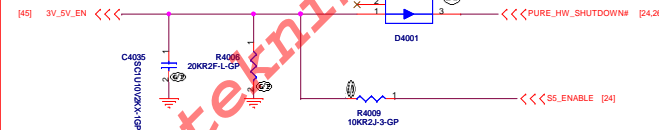
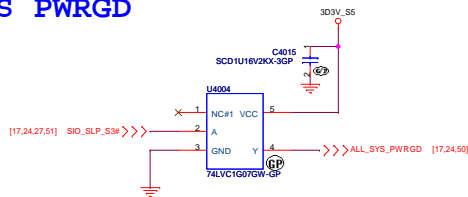
Power Good



VCCIO and VCCSTG

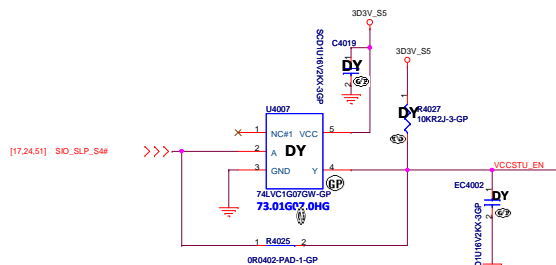


ALL SYS PWRGD

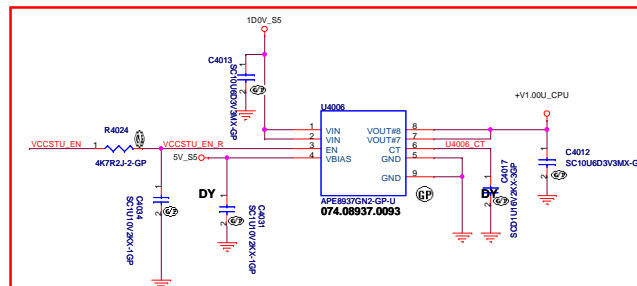


MANAGEMENT RAIL POWER GENERATION

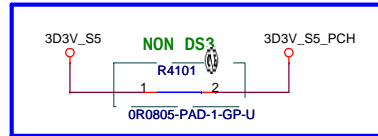
VCCST, VCCSTG, and VCCPLL remain powered during S4 and S5 power states for board VR optimization.



VCCST

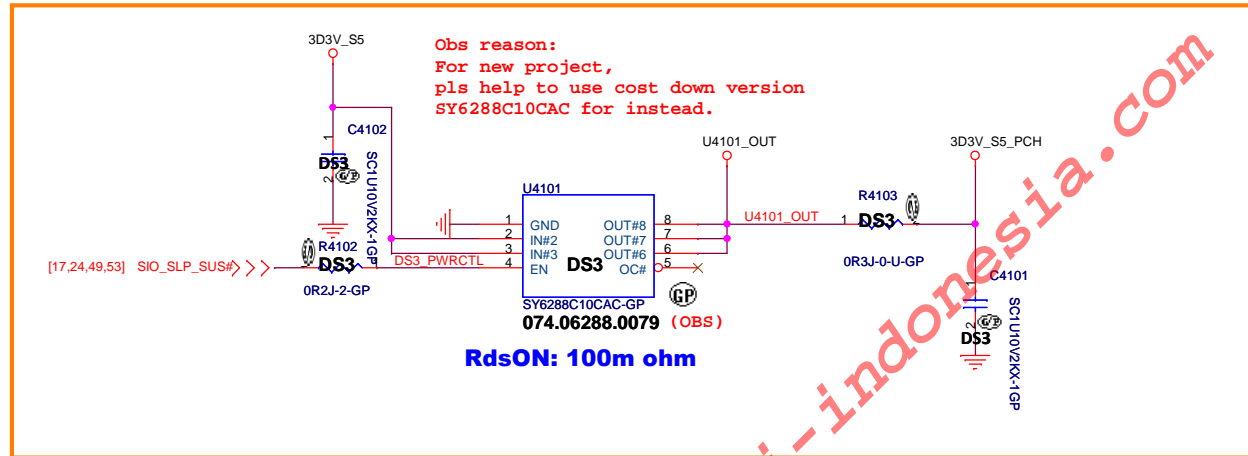


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Reserve by NON DS3 function 20150413

DS3



DS3

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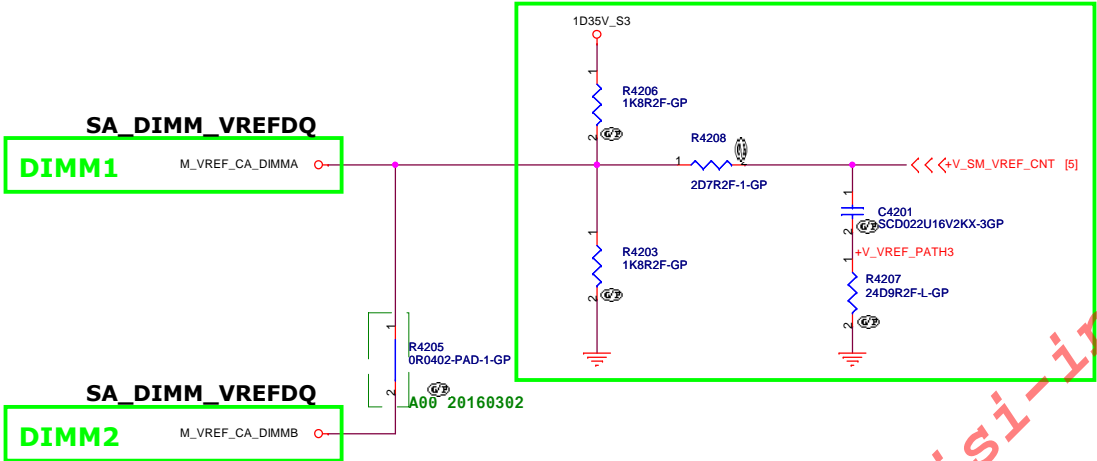
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Title		DS3	
Size	Document Number	Rev	
B	Drax KBL Y	A00	
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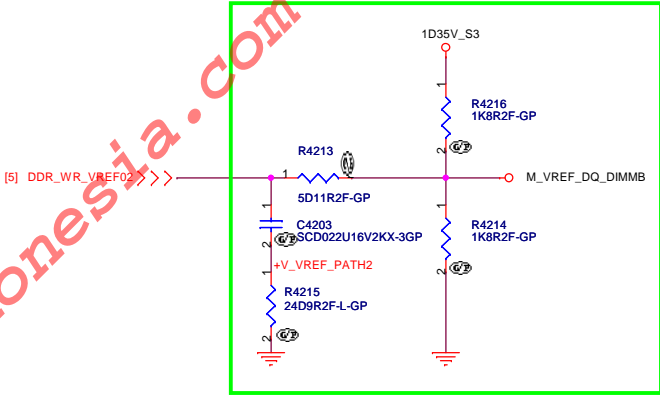
Main Func = DIMM1
Main Func = DIMM2

VREF CIRCUITRY

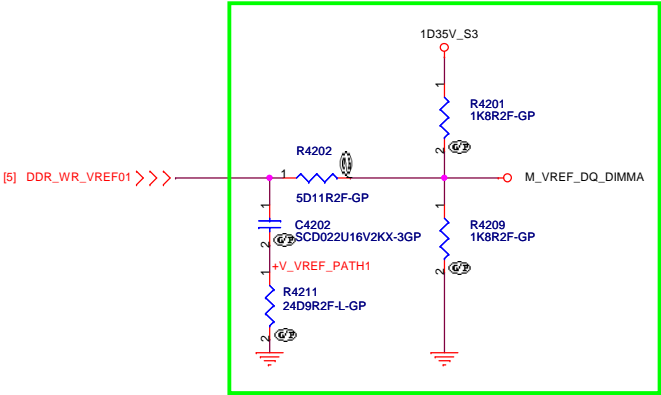
Layout Note:
Place Close DIMMs



Layout Note:
Place Close DIMM2



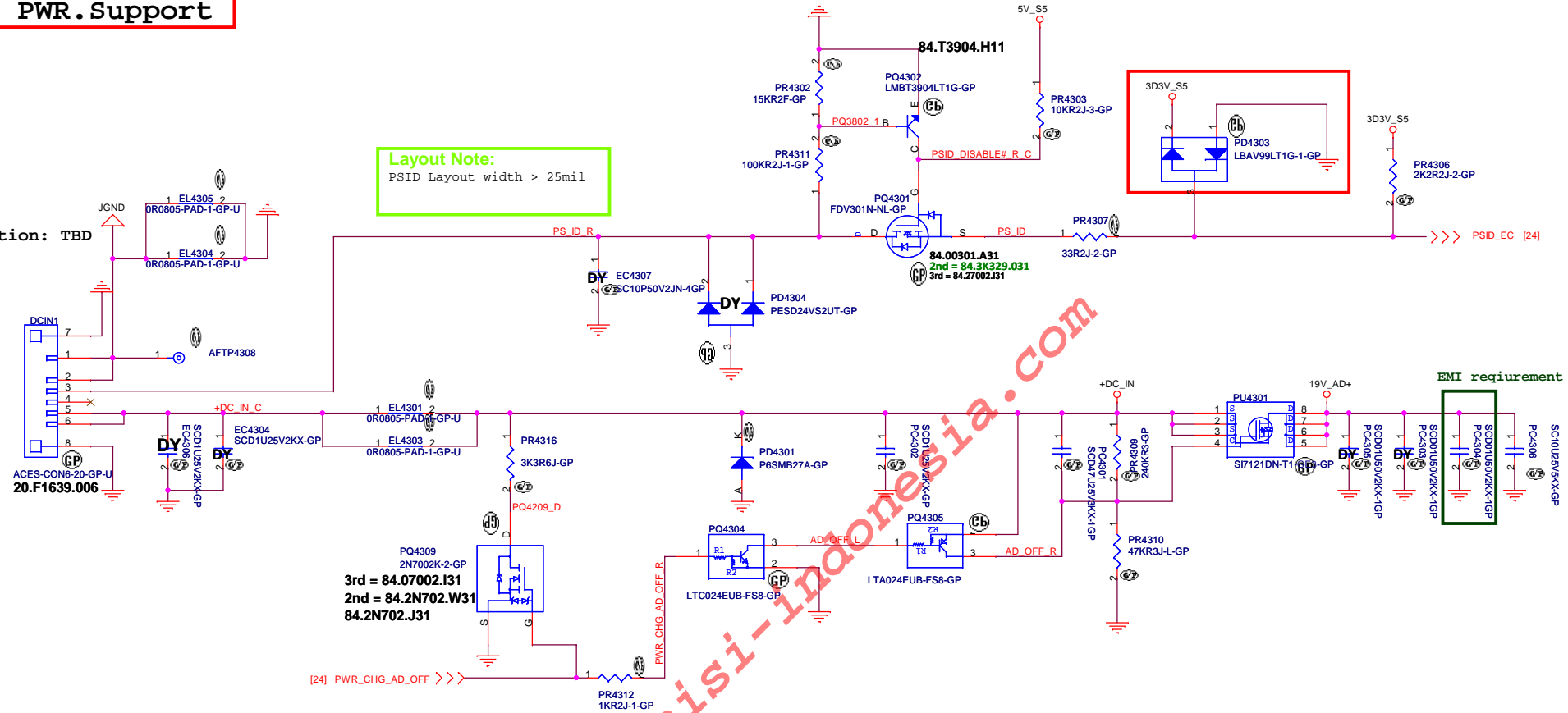
Layout Note:
Place Close DIMM1



SSID = PWR.Support

Pin Definition: TBD

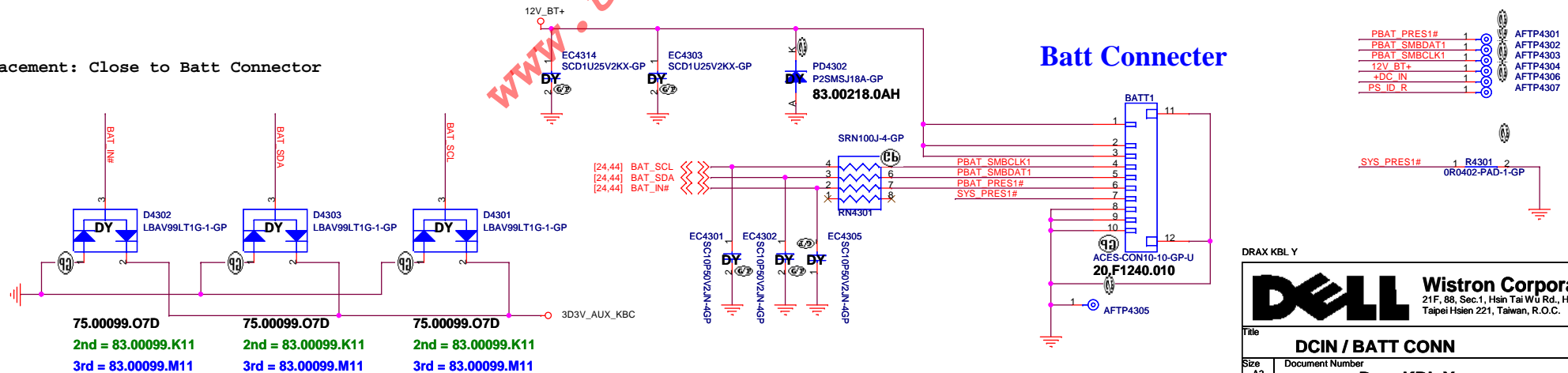
Layout Note:
PSID Layout width > 25mil



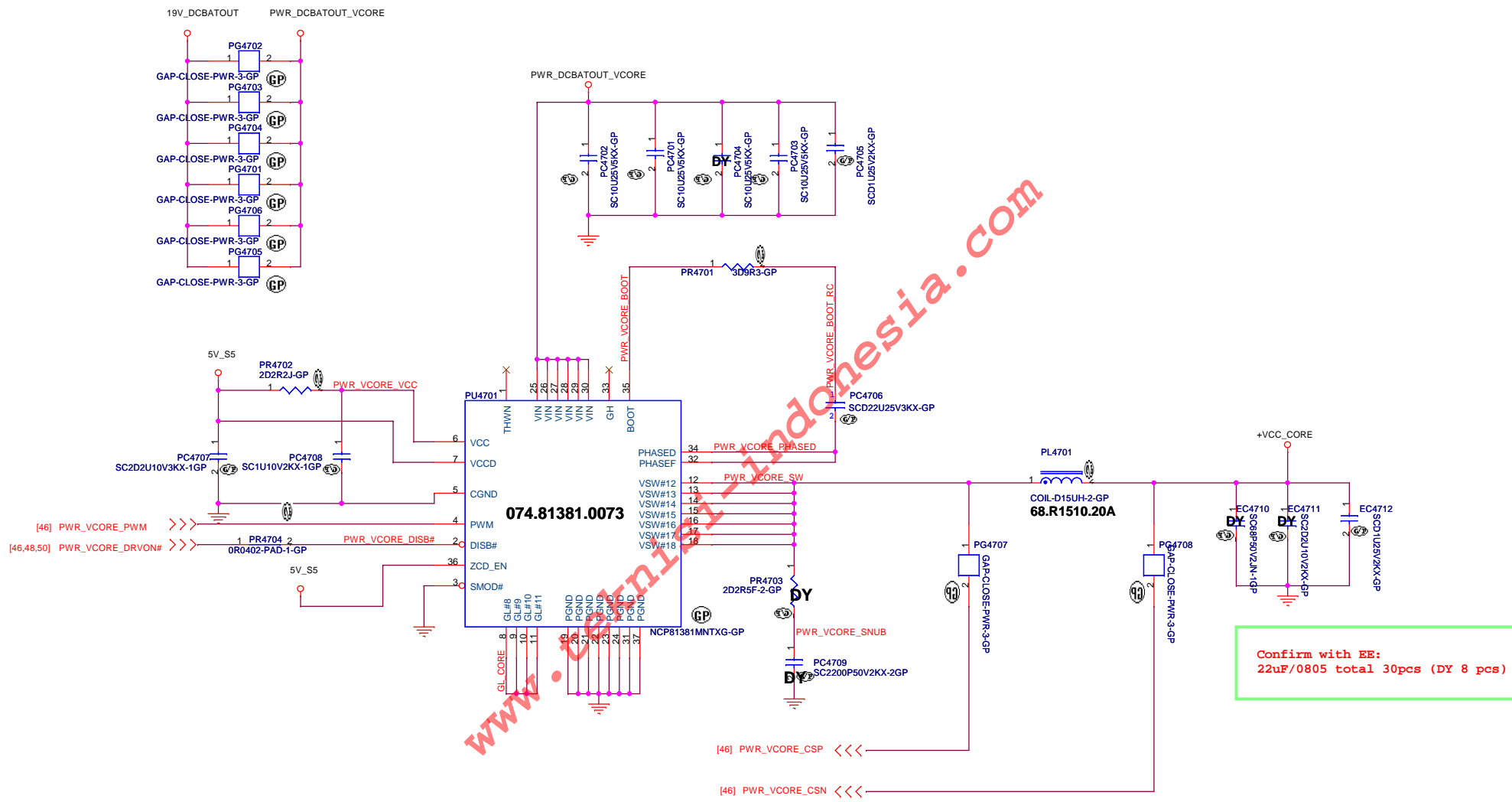
SSID = PWR.Support

Placement: Close to Batt Connector

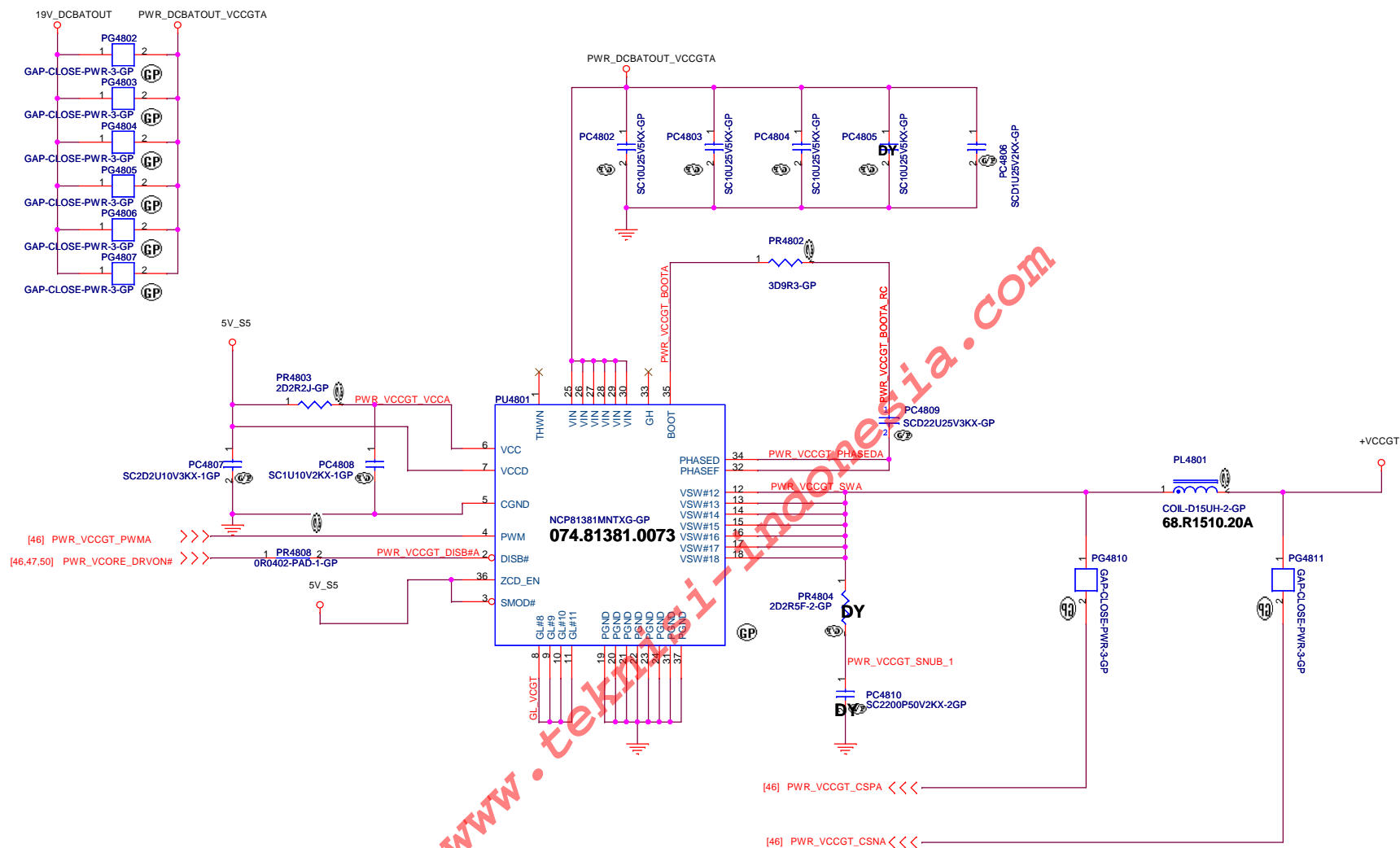
Batt Connector



Main Func = CPU_CORE



```
Main Func = CPU_CORE
```



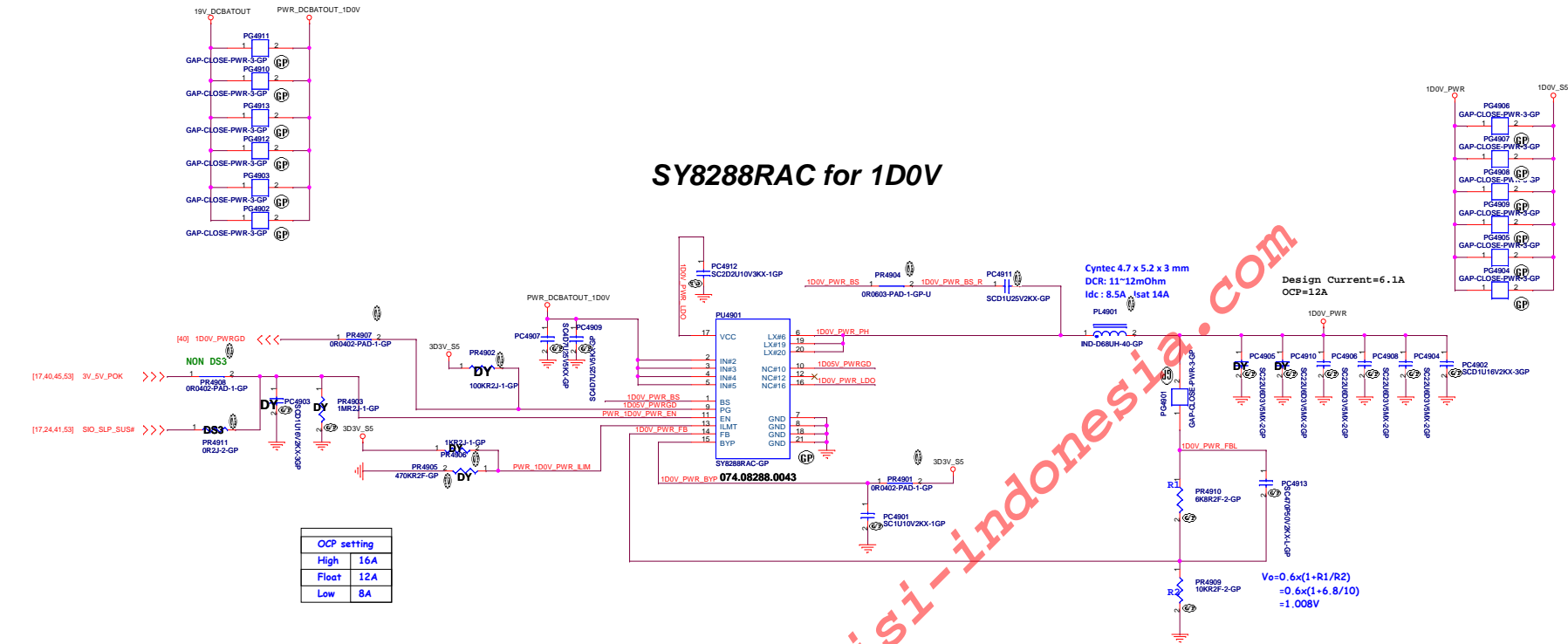
DRAX KBL Y



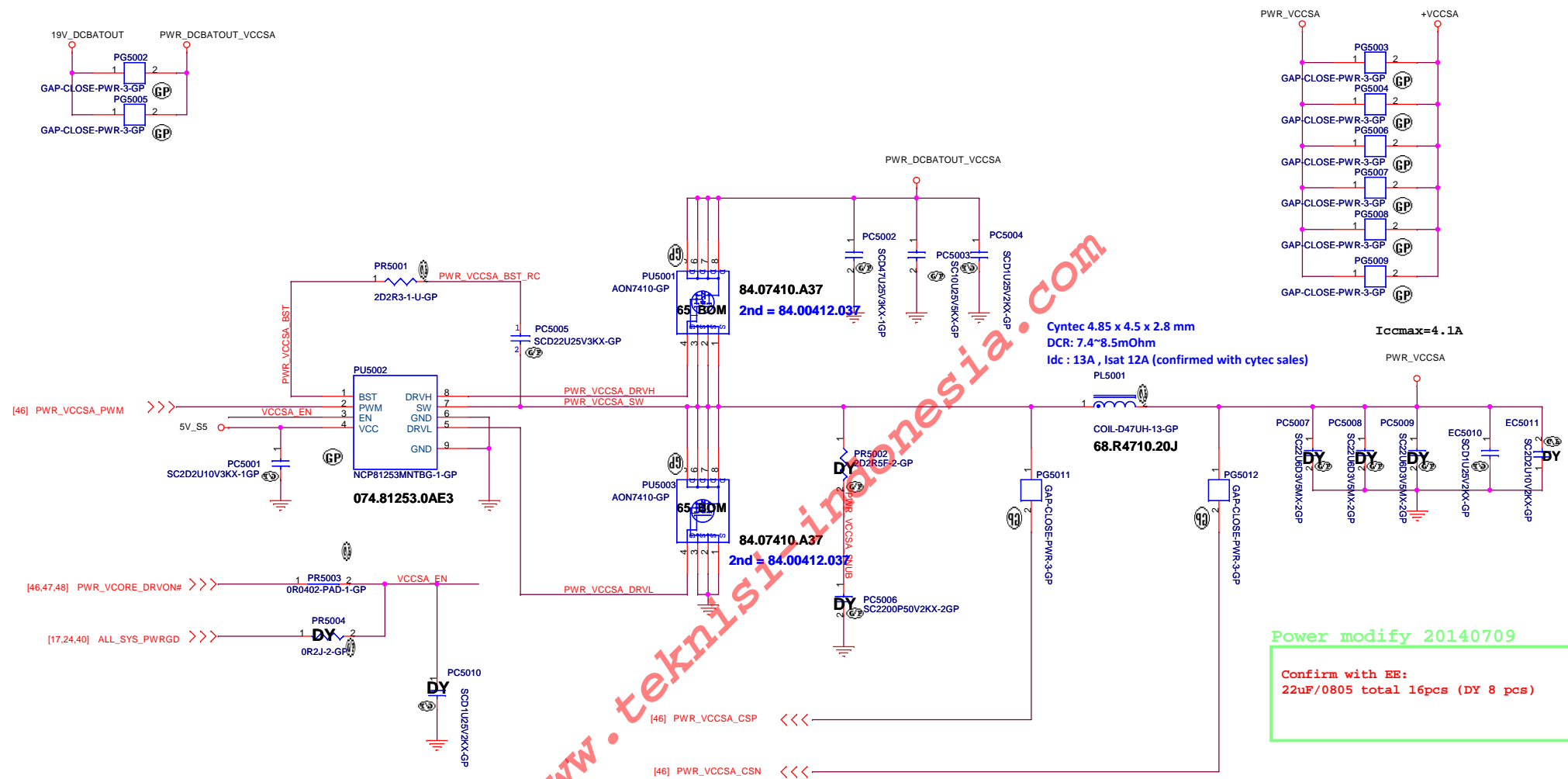
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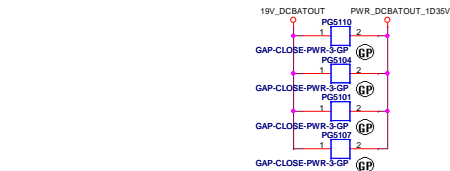
Title	NCP81201MNTXG_GFXCORE(3/3)
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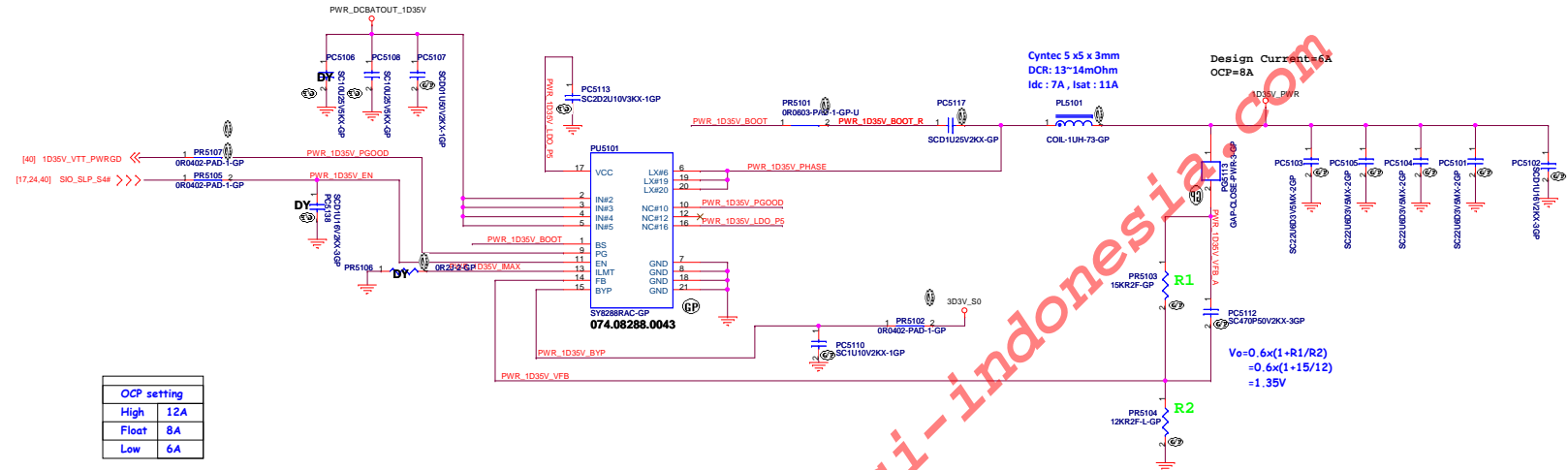


Main Func = CPU_CORE





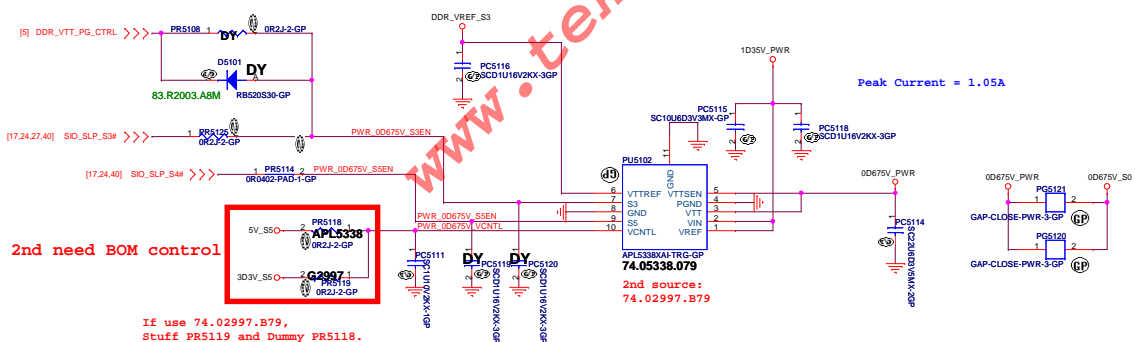
SY8288RAC for 1D35V



OCP setting	
High	12A
Float	8A
Low	6A

$$V_0 = 0.6 \times (1 + R1/R2)$$
$$= 0.6 \times (1 + 15/12)$$
$$= 1.35V$$

APL5338XAI for 0D675V



2nd need BOM control

If use 74.02997.B79,
Stuff PR5119 and Dummy PR5118.

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Title

S1339D15 1D5V

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A4

Document Number

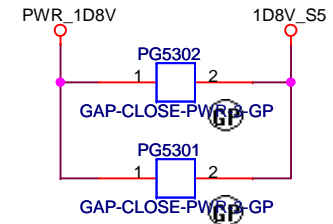
Drax KBL Y

Rev
A00

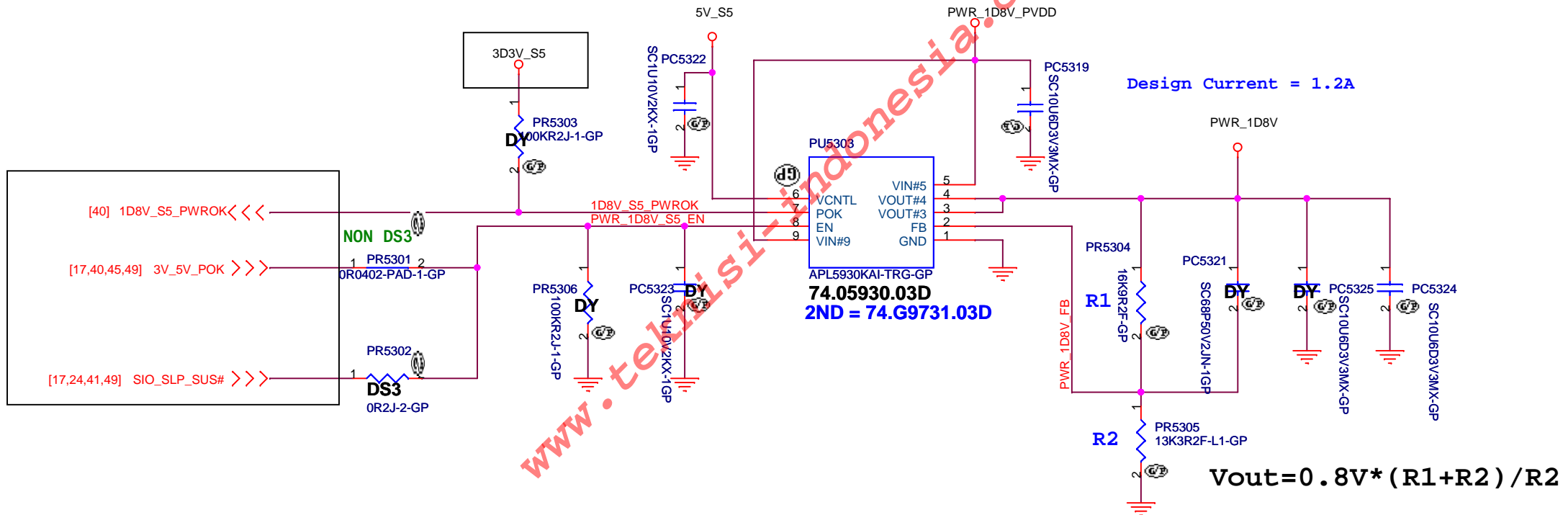
Date: Tuesday, June 28, 2016

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```
SSID = PWR.Plane.Regulator_1p8v
```



APL5930 for 1D8V_S5



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Title	SYW232 1D8V
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Size A4	Document Number Drax KBL Y	Rev A00
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Title

APL5930_1D24V

Size
A4

Document Number

Drax KBL Y

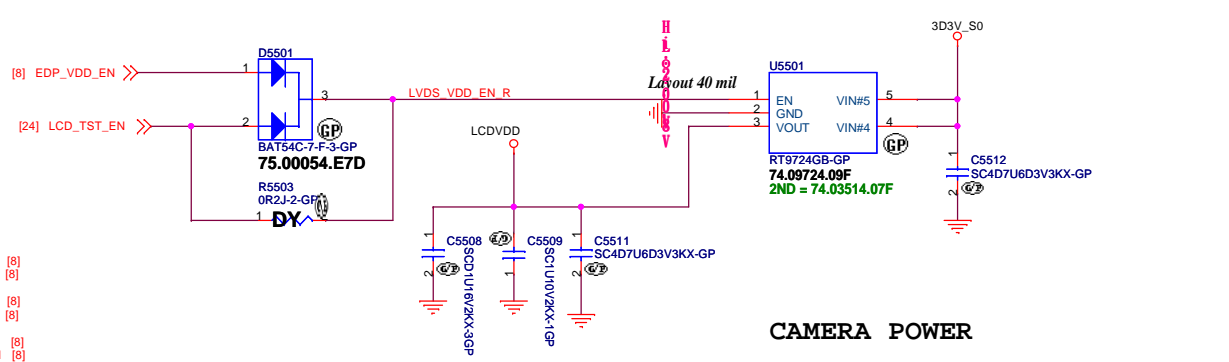
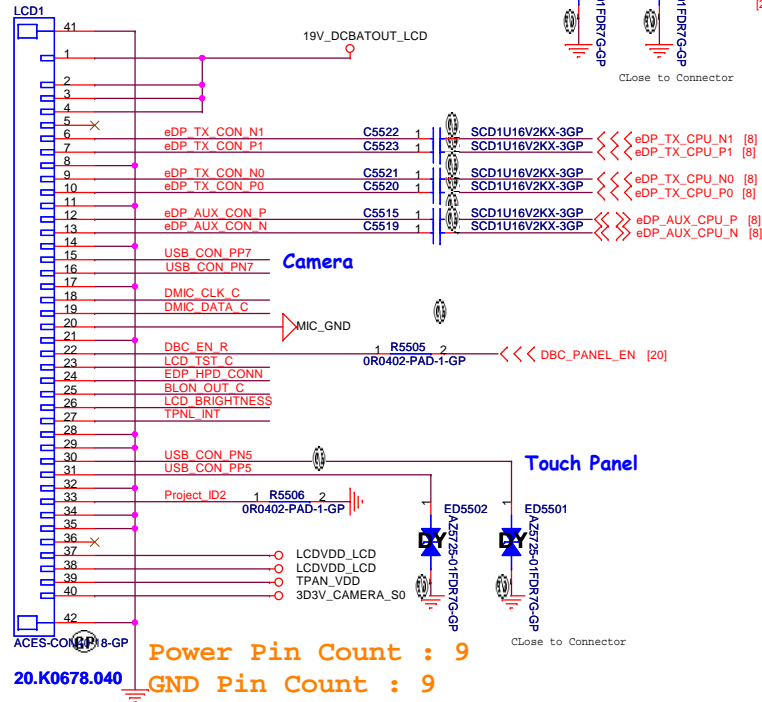
Rev
A00

Date: Tuesday, June 28, 2016

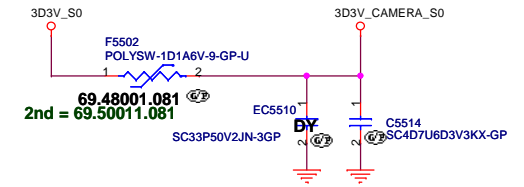
Sheet 54 of 109

SSID = VIDEO

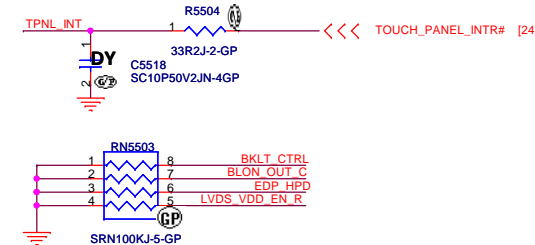
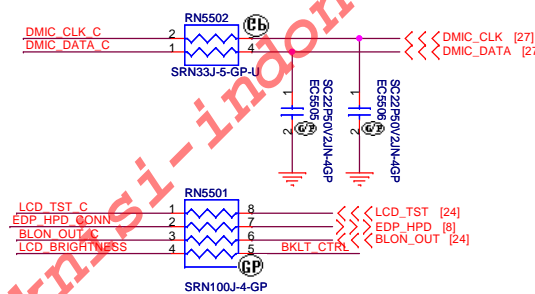
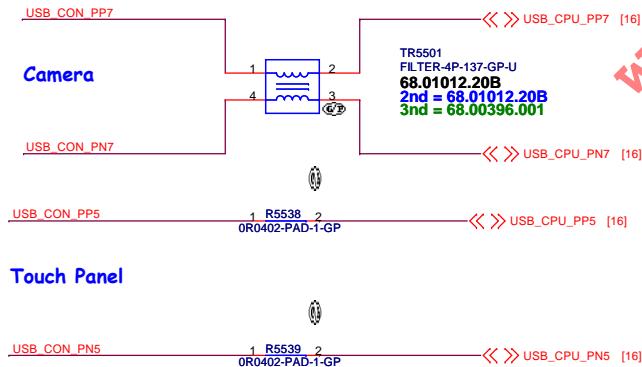
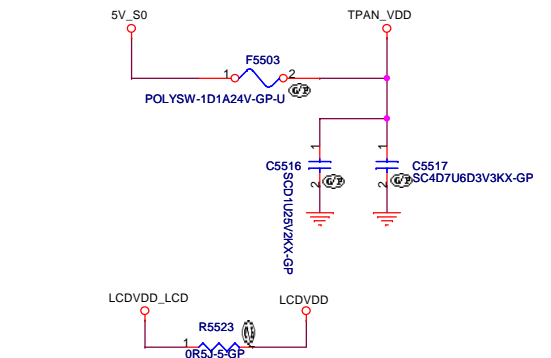
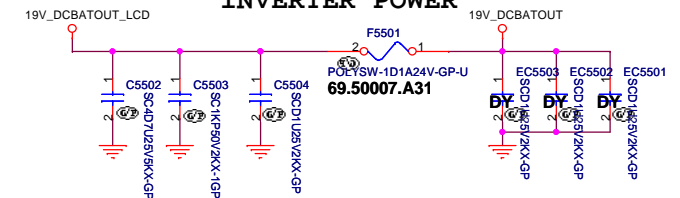
Panel Conn.



CAMERA POWER



INVERTER POWER



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DELL Wistron Corporation

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Title			HDMI Level Shifter/Connector
Size	Document Number	Rev	A00
A3	Drax KBL Y		
Date:	Tuesday, June 28, 2016	Sheet	55 of 109

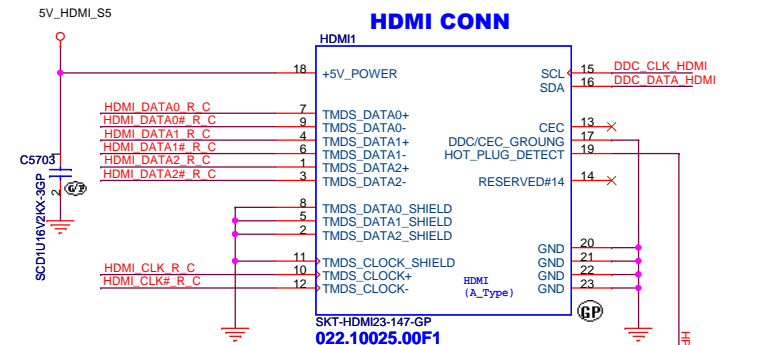
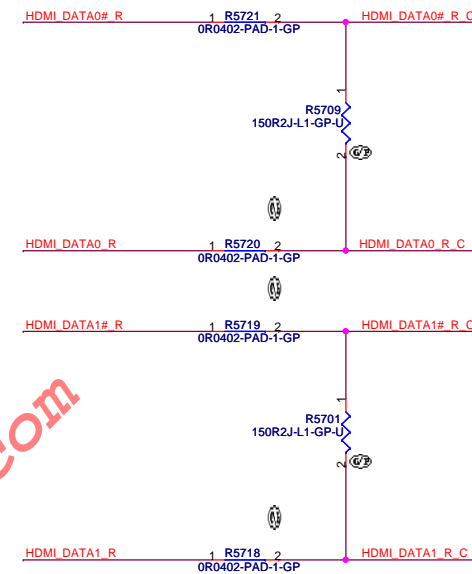
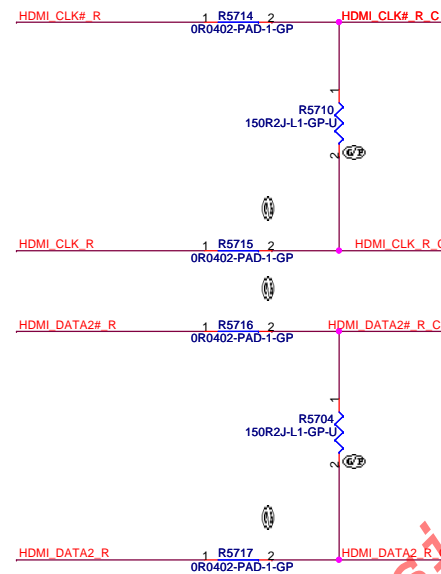
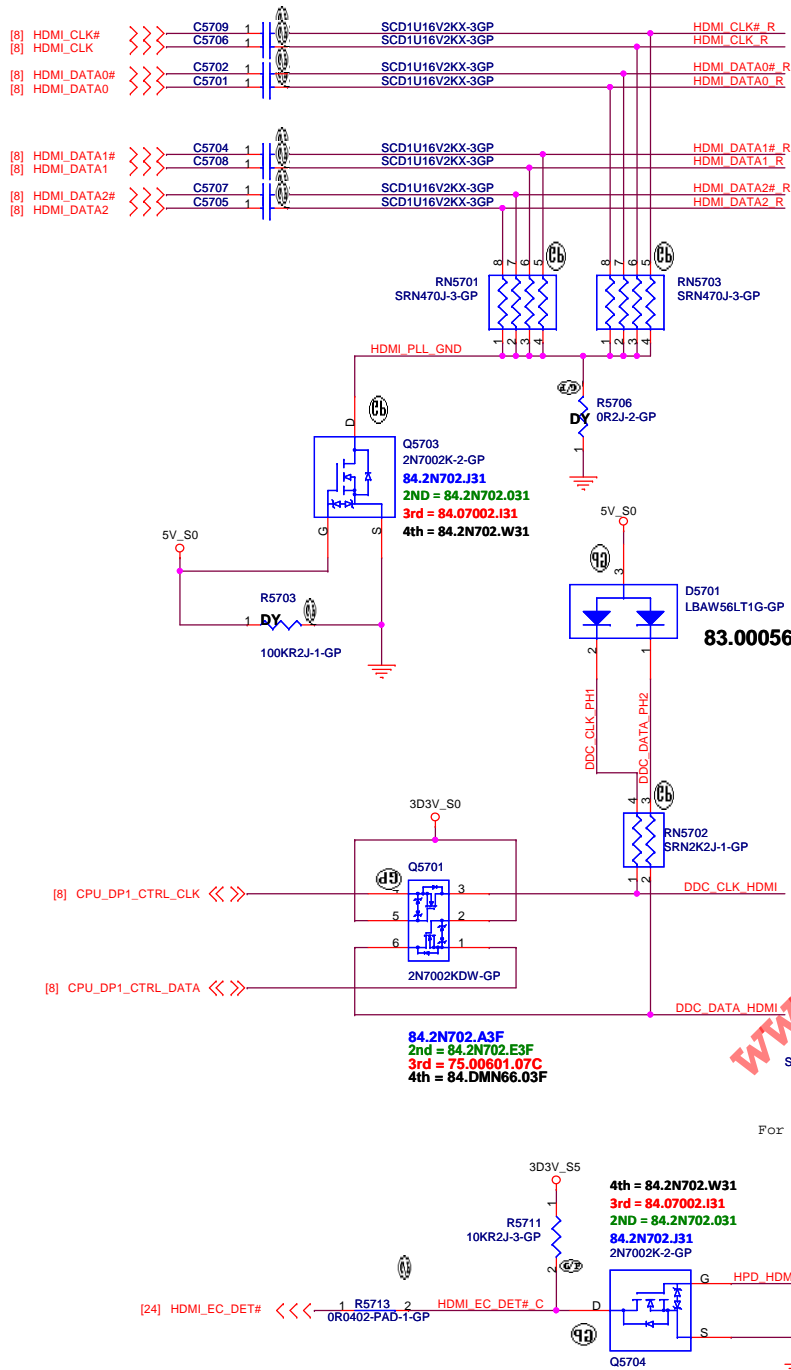
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Drax KBL Y		Rev A00
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SSID = VIDEO




SSID = Display Port

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Title

(Reserved) Display Port

Size

Document Number

Rev

Drax KBL Y

A00

Date: Tuesday, June 28, 2016

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SSID = DVI

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DRAX KBL Y



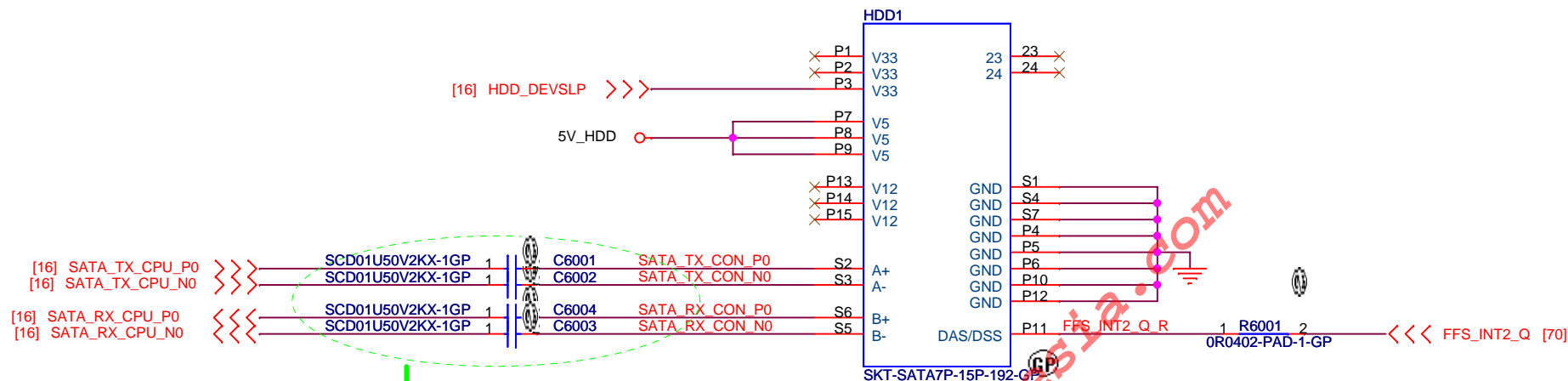
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **(Reserved) DVI**

Size	Document Number	Rev
	Drax KBL Y	A00

SSID = SATA

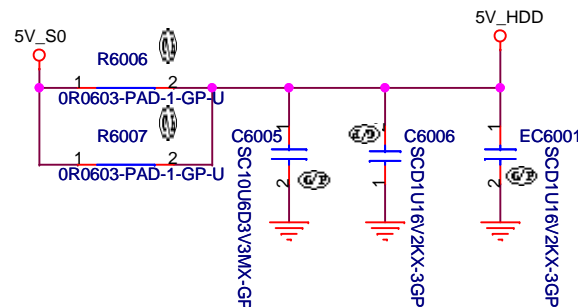
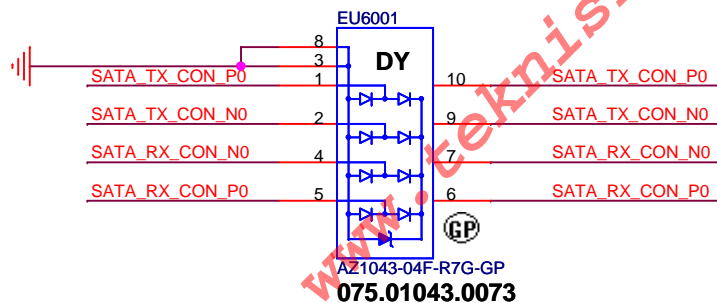
SATA HDD Connector



Layout Note :

AC coupling Cap;
place near CONN(<100mils)

022.10014.0081



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Title

HDD

Size

Document Number

Drax KBL Y

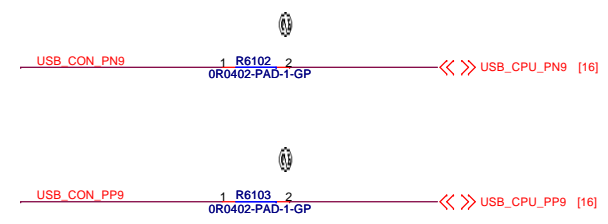
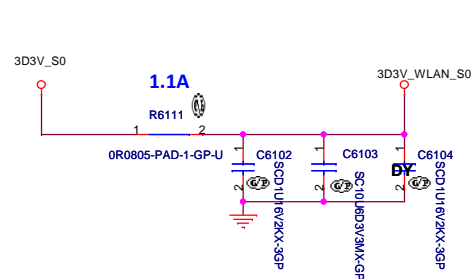
Rev

A00

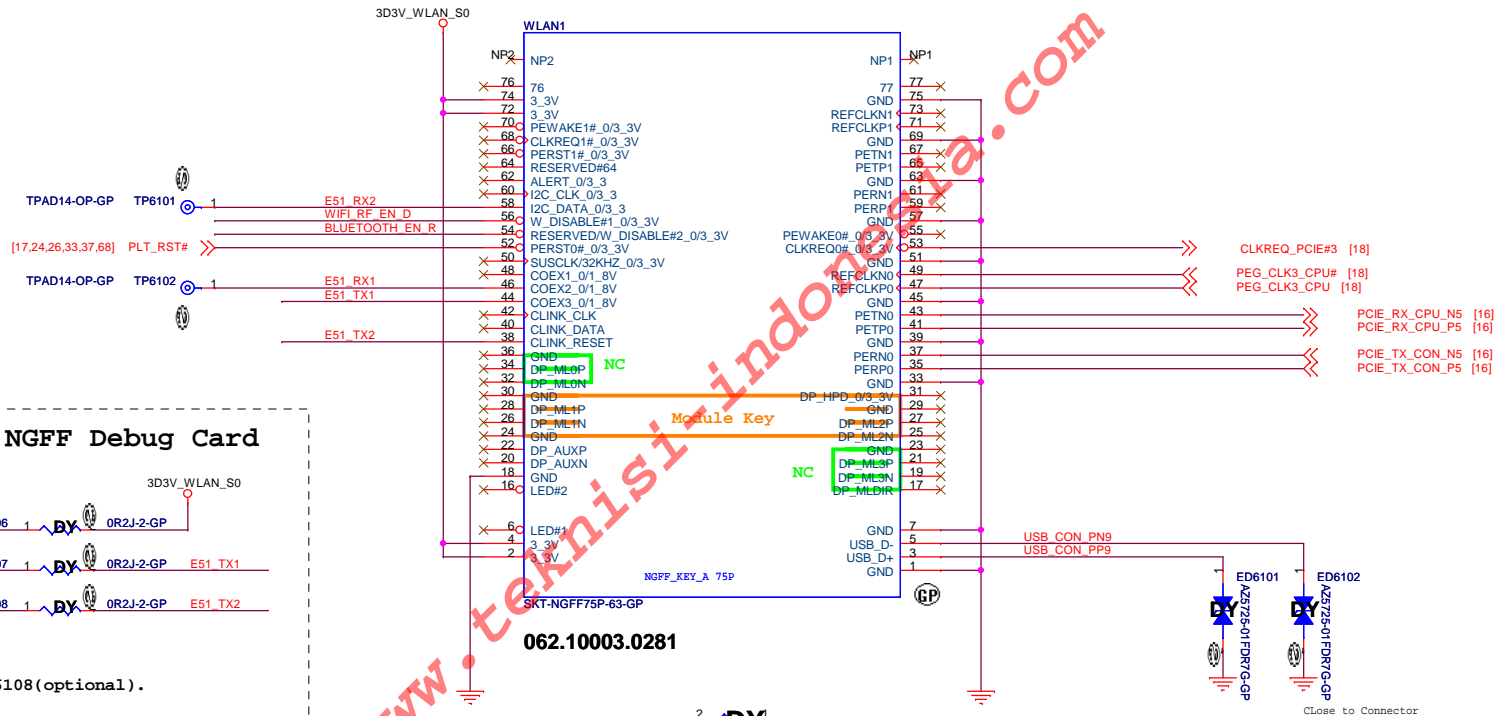
Date: Tuesday, June 28, 2016

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SSID = WLAN



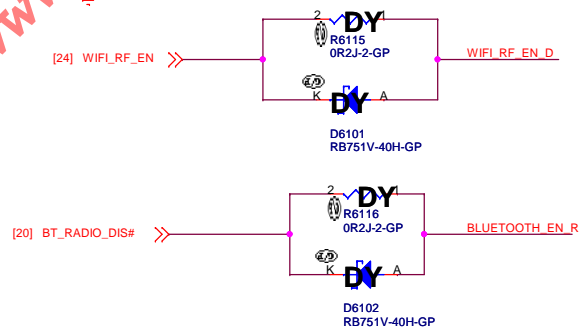
Mini Card Connector(802.11a/b/g)



Reserved for NGFF Debug Card

EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105

- 3D3V WLAN_S0
 - CLKREQ_PCIE#3
 - WIFI_RF_EN
 - PLT_RST#
 - BT_RADIO_DIS#
 - USB_CON_PP9
 - USB_CON_PN9
- TP6101
 - TP6102
 - TP6103
 - TP6104
 - TP6105
 - TP6106
 - TP6107



DRAX KBL Y

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Title: **WLAN**

Size	Document Number	Rev
	Drax KBL Y	A00

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SSID = WWAN

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Title		
(Reserved) WWAN		
Size	Document Number	Rev
	Drax KBL Y	A00
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SSID = SSD-NGFF

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Title eMMC			
Size A4	Document Number Drax KBL Y		Rev A00
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SSID = LED / PWRBTN

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Title

LED / PWRBTN

Size

A4

Document Number

Drax KBL Y

Rev

A00

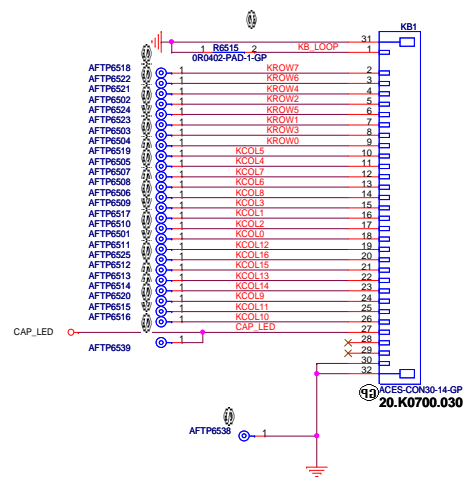
Date: Tuesday, June 28, 2016

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Main Func = KB

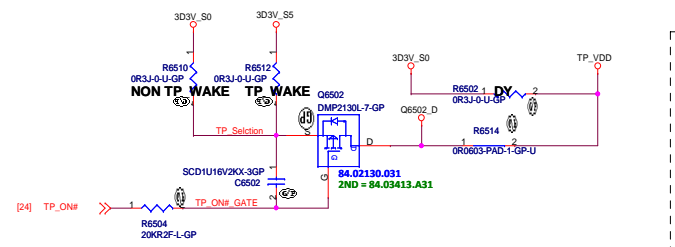
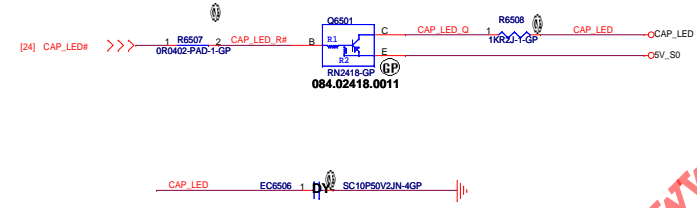
Main Func = TPAD

[24] KROW[0..7] >>>
[24] KCOL[0..16] <<<

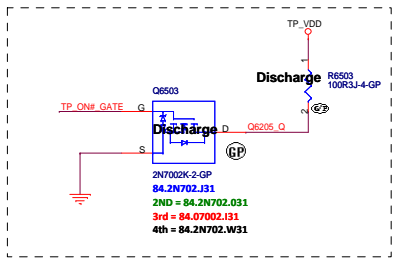


PIN#	SIGNAL
1	Diag_Loop-GPIO_I (TPC)
2	KSI [7] = KBD S8
3	KSI [6] = KBD S7
4	KSI [4] = KBD S5
5	KSI [2] = KBD S3
6	KSI [5] = KBD S6
7	KSI [1] = KBD S2
8	KSI [3] = KBD S4
9	KSI [0] = KBD S1
10	KSO [5] = KBD D6
11	KSO [4] = KBD D5
12	KSO [7] = KBD D8
13	KSO [6] = KBD D7
14	KSO [8] = KBD D9
15	KSO [3] = KBD D4
16	KSO [1] = KBD D2
17	KSO [2] = KBD D3
18	KSO [0] = KBD D1
19	KSO [12] = KBD D13
20	KSO [16] = KBD D17
21	KSO [15] = KBD D16
22	KSO [13] = KBD D14
23	KSO [14] = KBD D15
24	KSO [9] = KBD D10
25	KSO [11] = KBD D12
26	KSO [10] = KBD D11
27	CopsLock LED
28	N/C
29	N/C
30	GND

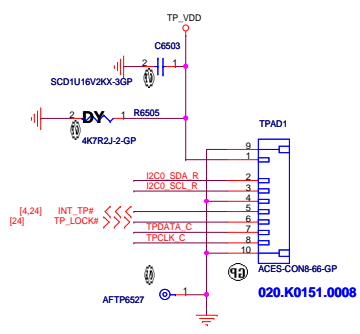
CAP LED Control
LOW acted from KBC GPIO



TP_VDD Discharge Circuit



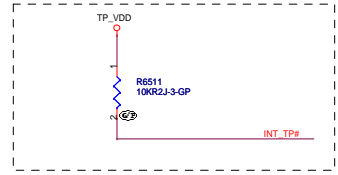
Touch Pad Connector



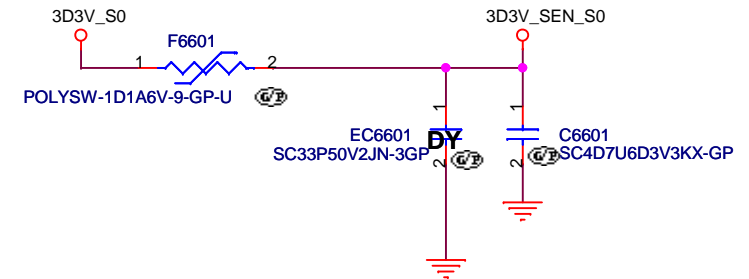
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

TP_VDD
TPCLK_C
TPDATA_C
I2C0_SCL_R
I2C0_SDA_R

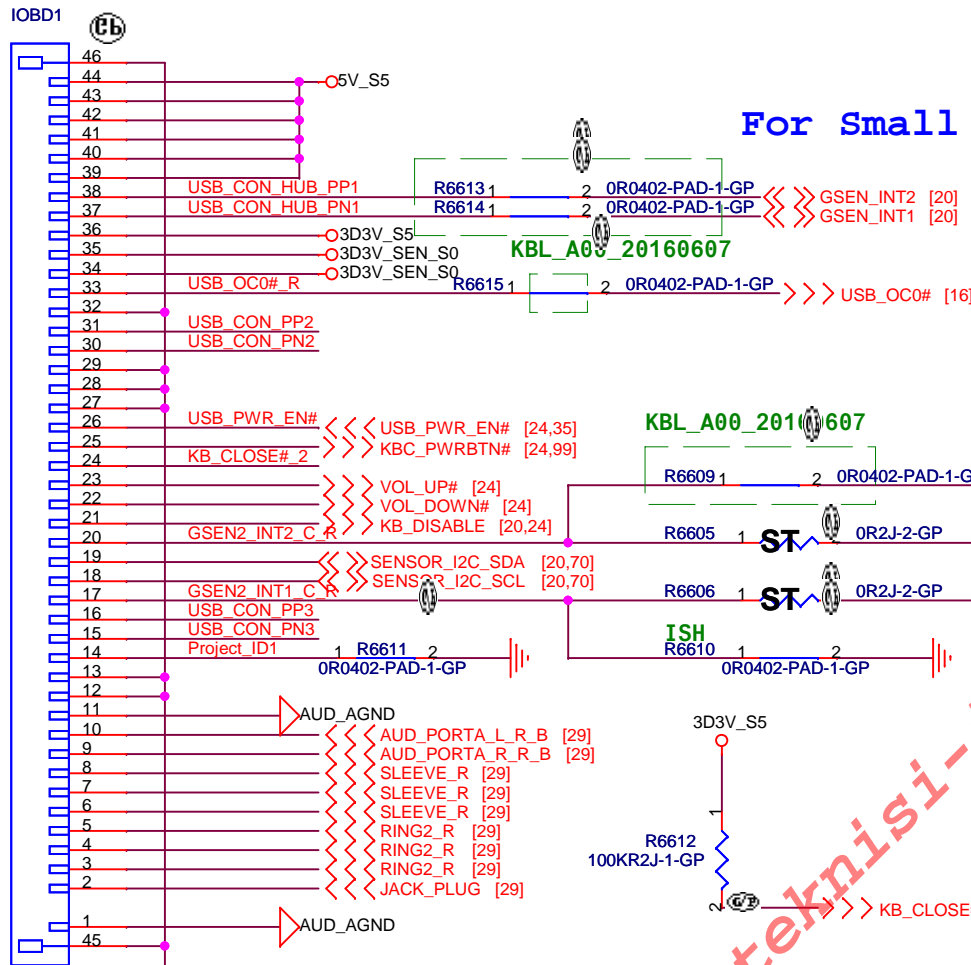
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



SENSOR POWER



For Small BD Sensor



Sensor HUB from USB HUB

USB2.0 Port2 from PCH

USB2.0 Port1 from USB HUB & PCH(Co-lay)

Power Pin Count : 8
GND Pin Count : 8


DRAX KBL Y

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board CONN			
Size A4	Document Number Drax KBL Y		Rev A00
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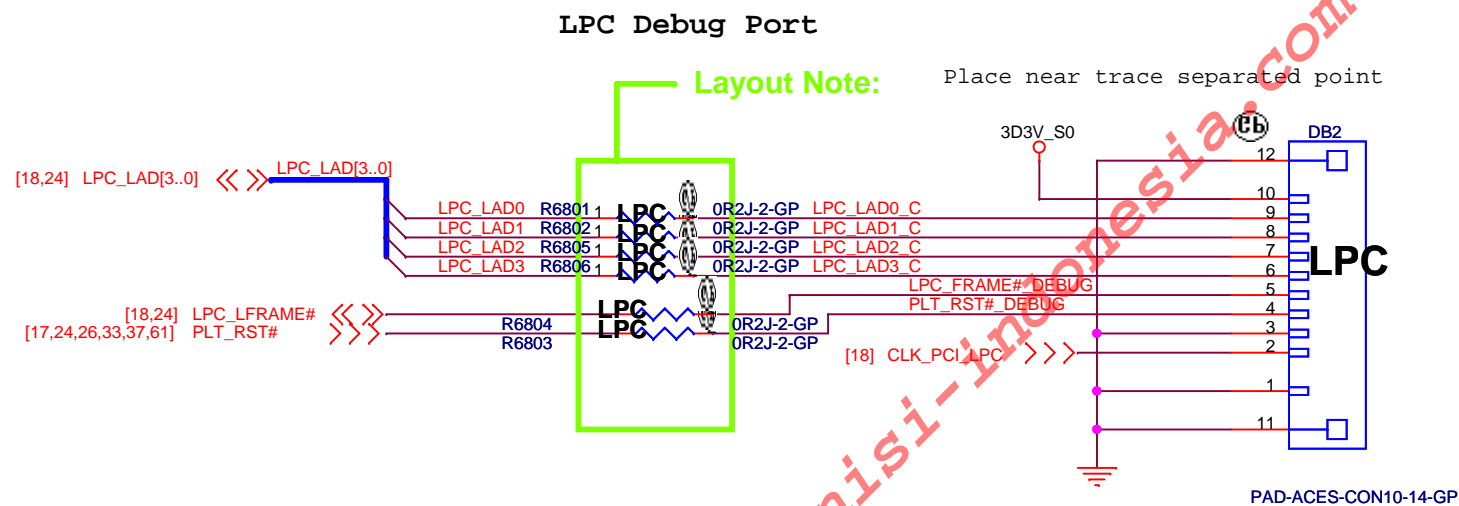
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Title			
Hall Sensor			
Size	Document Number		Rev
A4	Drax KBL Y		A00
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SSID = Debug CONN



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

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Title

Debug CONN

Size
A4

Document Number

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Rev

A00

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SSID = Sensor

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Title		
Sensor		
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Title **(Reserved)Thunderbolt (1/5)**

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Title **(Reserved)Thunderbolt (2/5)**

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Title **(Reserved)Thunderbolt (3/5)**

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Title **(Reserved)Thunderbolt (4/5)**

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Title **(Reserved)Thunderbolt (5/5)**

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Title **(Reserved)GPU (1/5) PEG**

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Title **(Reserved)GPU (2/5) DIGITAL**

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Title **(Reserved)GPU (3/5) VRAM**

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Title **(Reserved)GPU (4/5) GPIO**

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Title **(Reserved)GPU (5/5) PWR/GND**

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Title **(Reserved)VRAM1,2 (1/4)**

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Title **(Reserved)VRAM3,4 (2/4)**

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Title			(Reserved)VRAM5,6 (3/4)		
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Title **(Reserved)VRAM7,8 (4/4)**

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Title **(Reserved)VGA_CORE**

Size A4	Document Number Drax KBL Y	Rev A00
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Title **(Reserved)DISCRETE VGAPOWER**

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Title

(Reserved)

Size
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Title			(Reserved)		
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A4	Drax KBL Y				A00
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Main Func = UnusedParts

34.34S02.002
SPRING-98-GP
SPR1
Spring

34.41Y19.001
SPRING-12-GP-U1
SPR5
Spring

34.41Y19.001
SPRING-12-GP-U1
SPR6
Spring

34.40X45.101
HS1
STF237R117H67-3-GP

34.40X45.101
HS2
STF237R117H67-3-GP

34.40X45.101
HS3
STF237R117H67-3-GP

34.40X45.101
HS4
STF237R117H67-3-GP

34.4SE26.001
HS5
STF237R113H62-4-GP

H1
HOLE256R142-OG-1-GP
ZZ.00PAD.6U1

H2
HOLE335R197-GP
ZZ.00PAD.7L1

H3
HOLE335R197-GP
ZZ.00PAD.7L1

H4
HOLE335R197-GP
ZZ.00PAD.7L1

Package symbol : GNDPADSR335-213-S
G1803
GNDPAD
ZZ.NDPAD.XXX
TOP
G1804
GNDPAD
ZZ.NDPAD.XXX
BOTTOM

Main Func = EMICapacitors

19V_DCBATOUT
acoustic noise
DY PT8902
SE33U25VM-11-GP
DY PT8903
SE33U25VM-11-GP

19V_DCBATOUT
DY FC8901 SCD1U25V2KX-GP
DY FC8902 SCD1U25V2KX-GP
DY FC8903 SCD1U25V2KX-GP
DY FC8904 SCD1U25V2KX-GP
DY FC8905 SCD1U25V2KX-GP
DY FC8906 SCD1U25V2KX-GP
DY FC8907 SCD1U25V2KX-GP
DY FC8908 SCD1U25V2KX-GP
DY FC8909 SCD1U25V2KX-GP
DY FC8910 SCD1U25V2KX-GP
DY FC8911 SCD1U25V2KX-GP
DY FC8912 SCD1U25V2KX-GP
DY FC8913 SCD1U25V2KX-GP
DY FC8914 SCD1U25V2KX-GP
DY FC8915 SCD1U25V2KX-GP
DY FC8916 SCD1U25V2KX-GP
DY FC8917 SCD1U25V2KX-GP
DY FC8918 SCD1U25V2KX-GP
1D35V_S3
Near PR4652
0D675V_S0
Near C1329
+VCC_CORE
+VCCGT
19V_DCBATOUT_LCD

RF Reserved

19V_DCBATOUT
DY FC8901 SCD1U25V2KX-GP
DY FC8902 SCD1U25V2KX-GP
DY FC8903 SCD1U25V2KX-GP
DY FC8904 SCD1U25V2KX-GP
DY FC8905 SCD1U25V2KX-GP
DY FC8906 SCD1U25V2KX-GP
DY FC8907 SCD1U25V2KX-GP
DY FC8908 SCD1U25V2KX-GP
DY FC8909 SCD1U25V2KX-GP
DY FC8910 SCD1U25V2KX-GP
DY FC8911 SCD1U25V2KX-GP
DY FC8912 SCD1U25V2KX-GP
DY FC8913 SCD1U25V2KX-GP
DY FC8914 SCD1U25V2KX-GP
DY FC8915 SCD1U25V2KX-GP
DY FC8916 SCD1U25V2KX-GP
DY FC8917 SCD1U25V2KX-GP
DY FC8918 SCD1U25V2KX-GP
EMI Reserved

5V_S0
Near TPAD1
5V_S0
Near SPI252
3D3V_S5_PCH
Near R6509
PWR_DCBATOUT_5V
Near R2513
3D3V_S5
Near PR4512
Near PC4810
RF Reserved

DRAX KBL Y


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
UNUSED PARTS/EMI Capacitors		
Size A3	Document Number Drax KBL Y	Rev A00
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)NFC Connector			
Size A4	Document Number Drax KBL Y		Rev A00
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Title (Reserved) TPM			
Size A4	Document Number Drax KBL Y		Rev A00
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Finger Print			
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Title (Reserved)Express Card		
Size A4	Document Number Drax KBL Y	Rev A00
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Title			(Reserved)Smart Card Socket		
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Title **(Reserved)SW GFX eDP**

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SSID = DEBUG PORT

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Title				CPU XDP			
Size	A4	Document Number			Rev		
		Drax KBL Y			A00		
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Title

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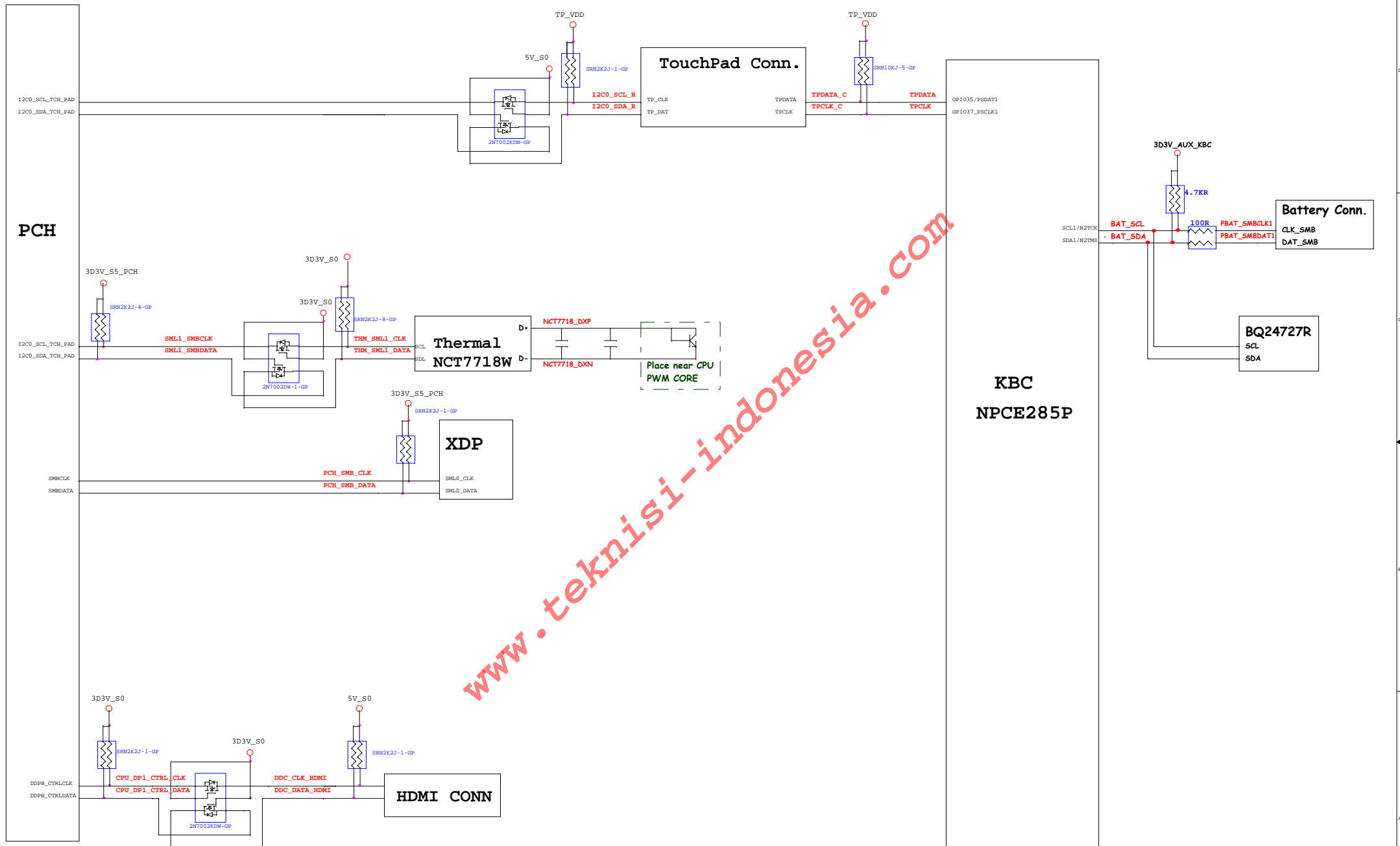
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **(Reserved)LAN SWITCH**

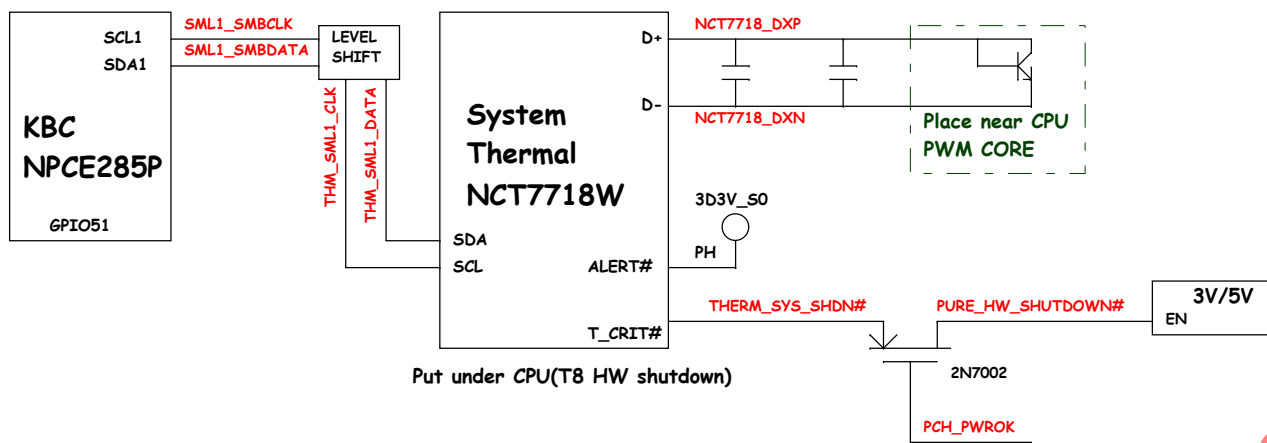
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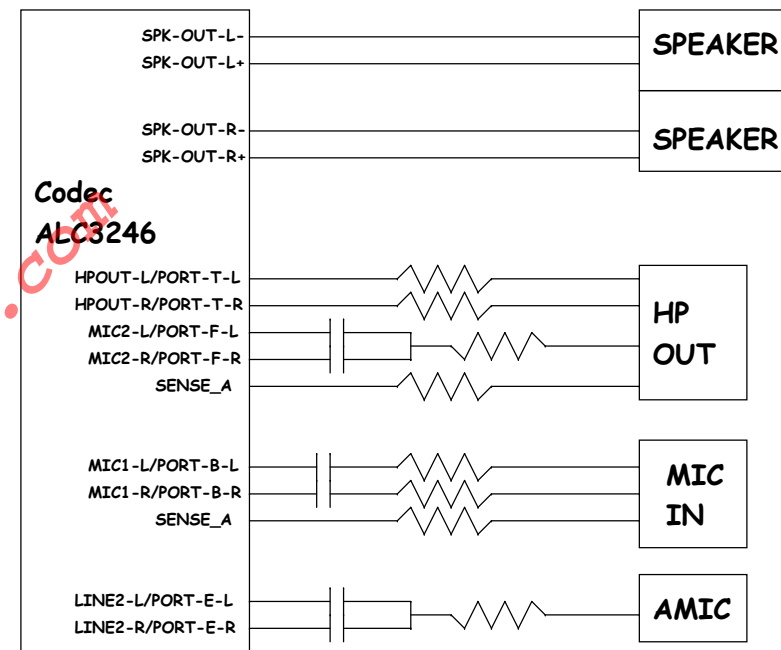
SMBus Block Diagram



Thermal Block Diagram




Audio Block Diagram



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